Reasoning about Translation Lookaside Buffers (TLBs)

LPAR-21

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Trustworthy Systems @ Data61

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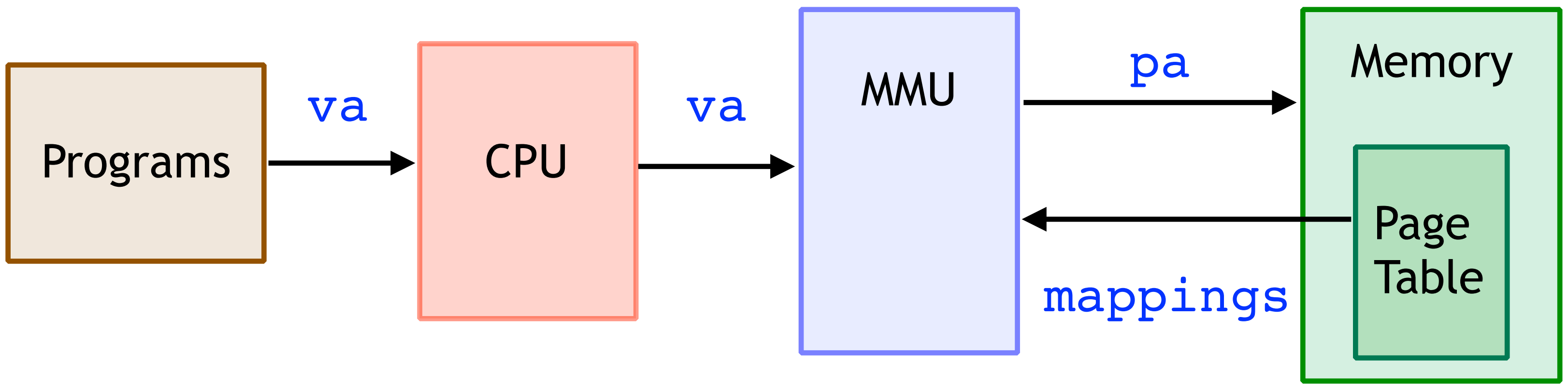
What is a TLB



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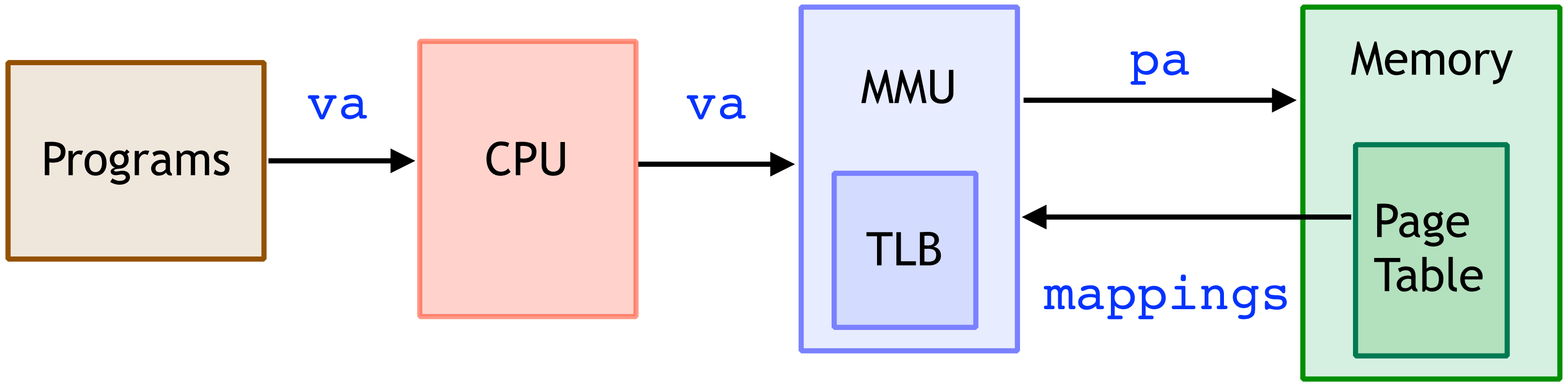

- TLB
  - dedicated cache for page table walks
  - architecture specific

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- Extend seL4 program logic for TLB reasoning
  - a formal TLB model for ARMv7 architecture

Contributions

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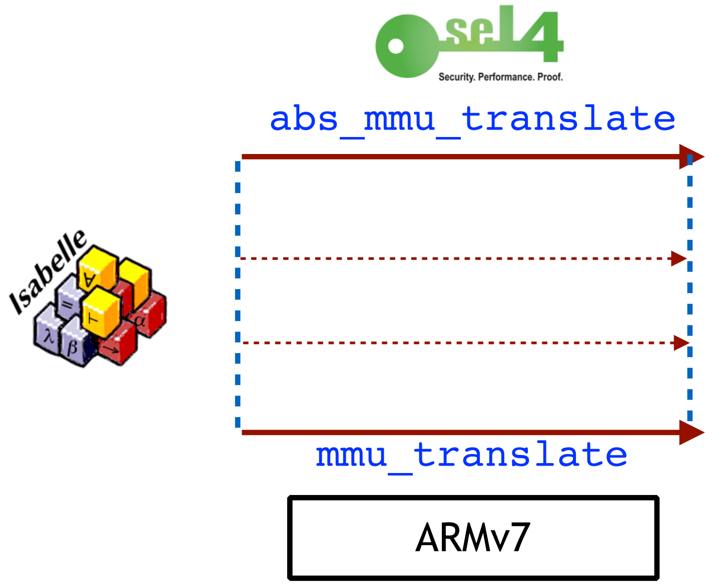

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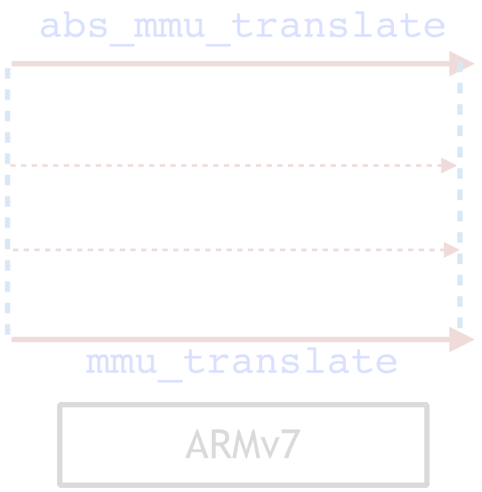
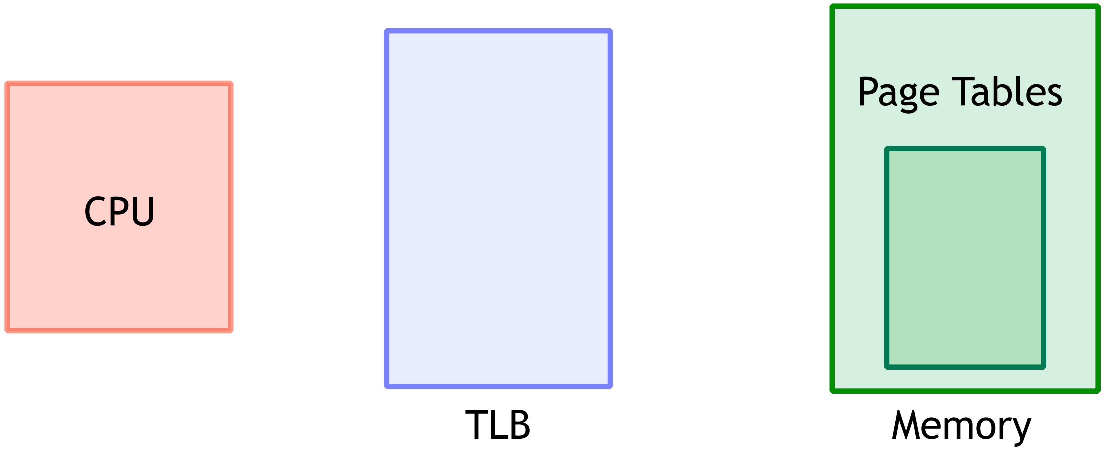


ARMv7-style TLB



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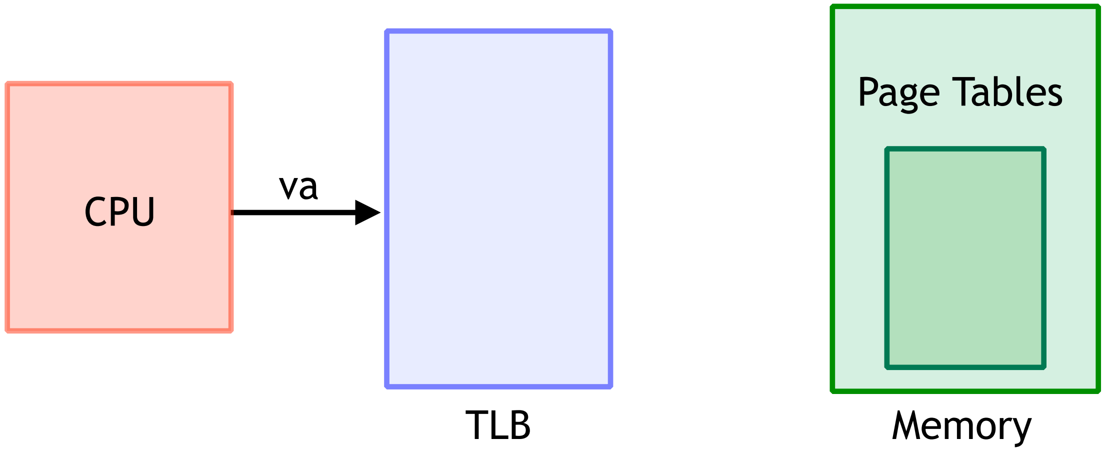

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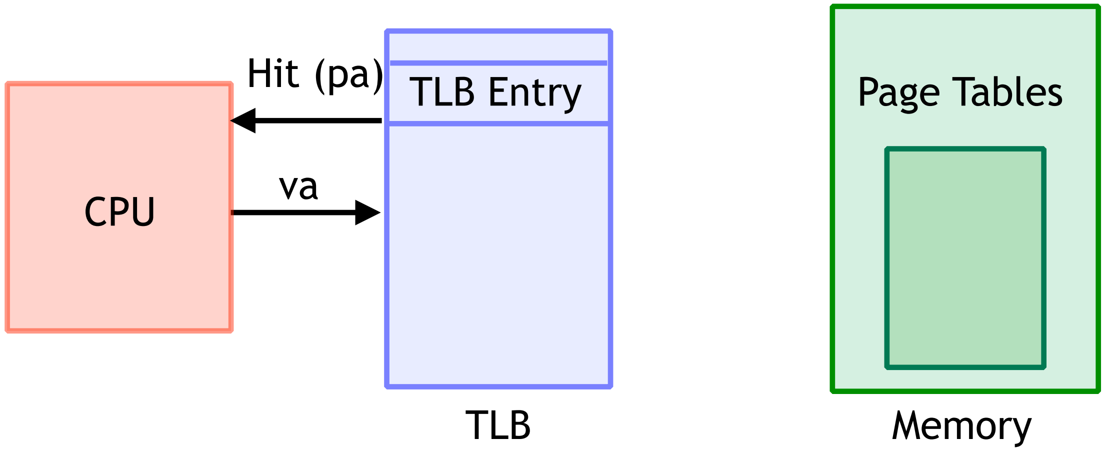

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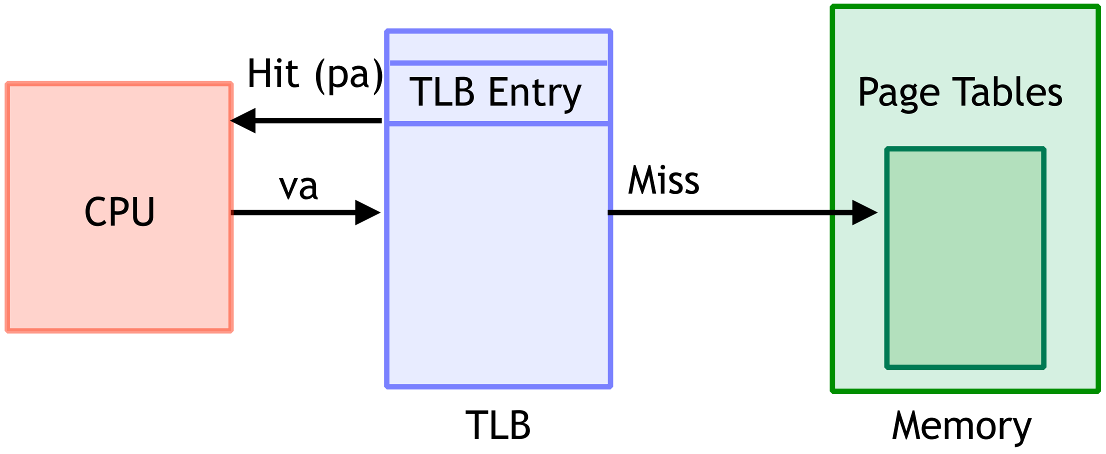

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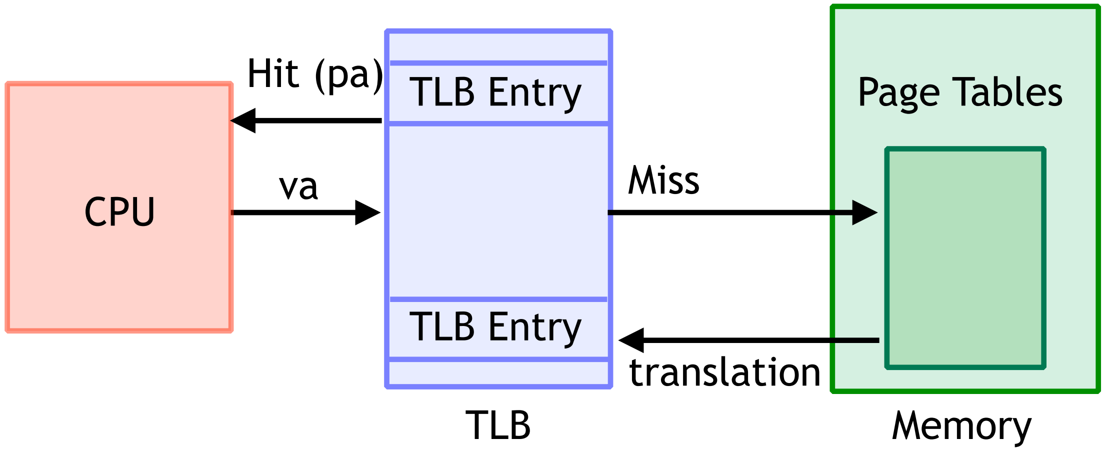

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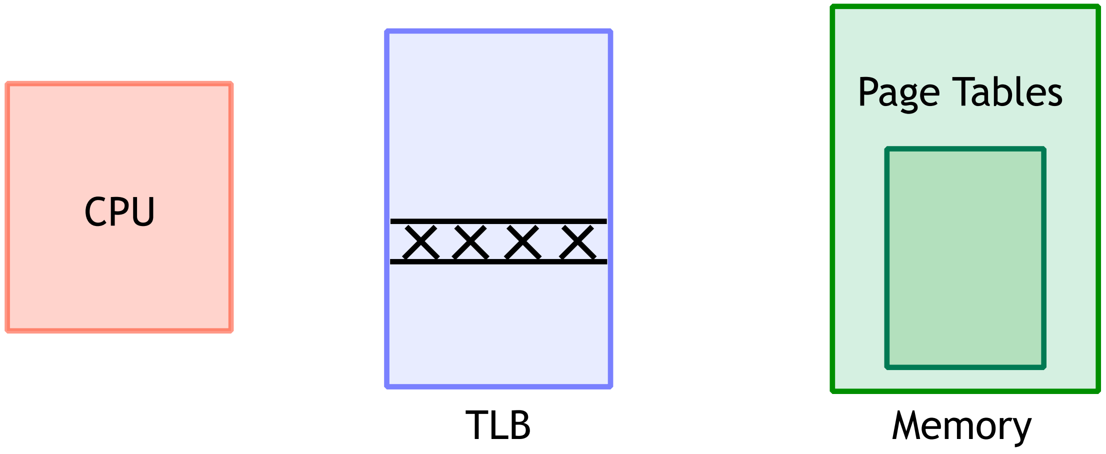

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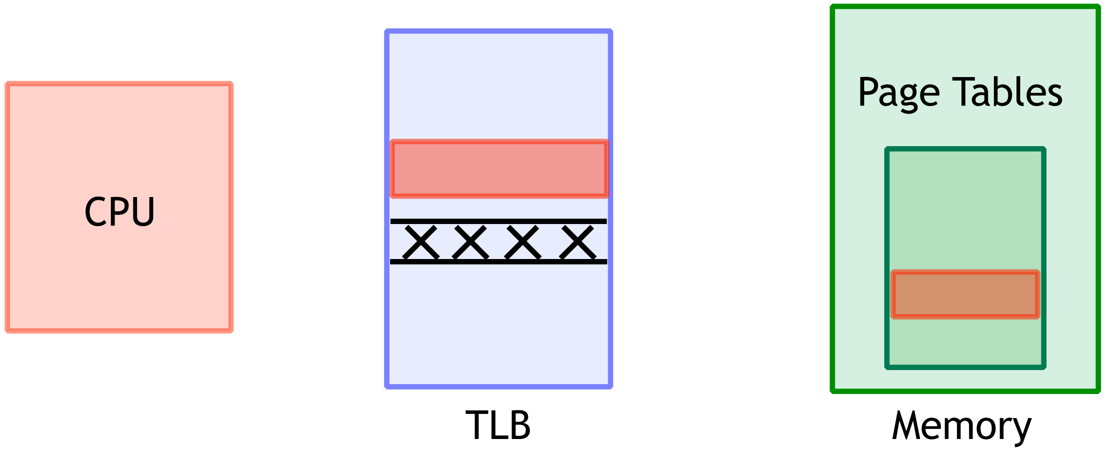

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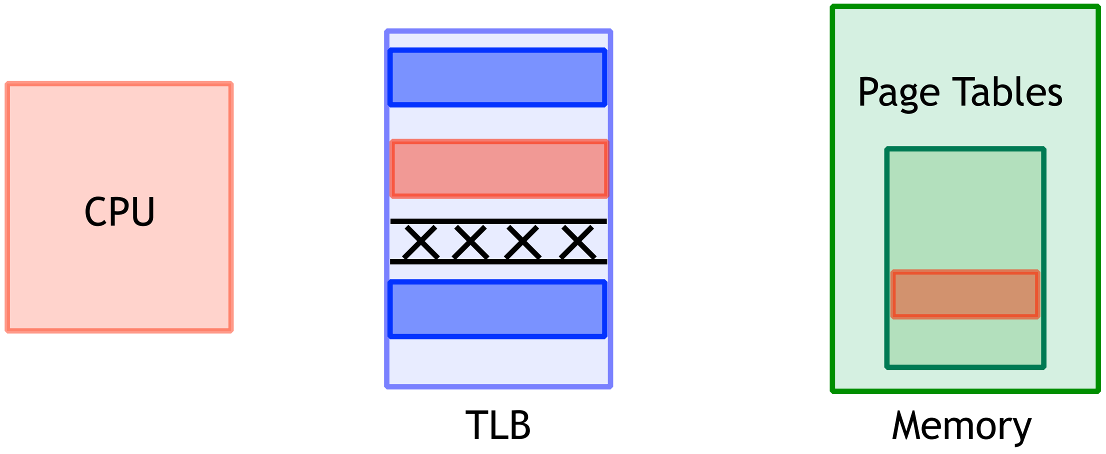

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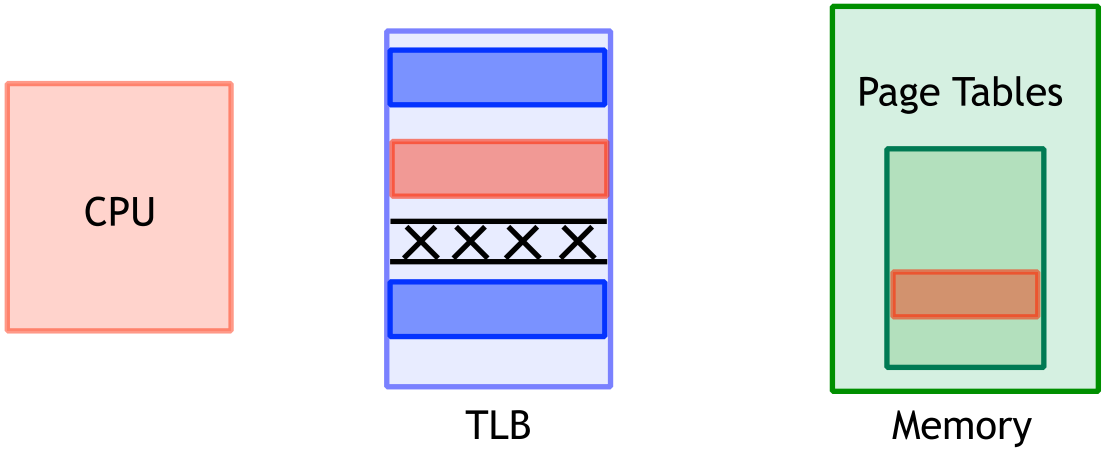

- TLB maintenance operations
  - flush entries after write to page table
  - lazy invalidation
    - Address Space IDentifier - ASID

ARMv7-style Formal Model of TLB

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lookup :: tlb ⇒ asid ⇒ vaddr ⇒ lookup_type
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flush operations
- selective_invalidation
- asid_invalidation
- va_invalidation

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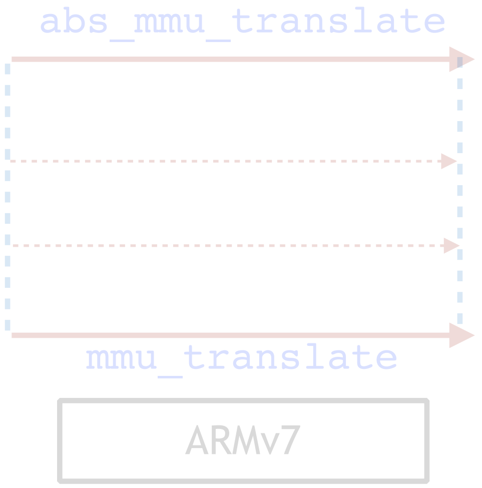

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- `mmu_translate` function
- Update `mem_write` and `mem_read` functions
- Virtualize the subsequent memory accesses

MMU and Memory Functions

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  (mem, asid, ttbr0, tlb) ← read_state (MEM, ASID, TTBR0, tlb);
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    let entry = pt_walk asid mem ttbr0 va
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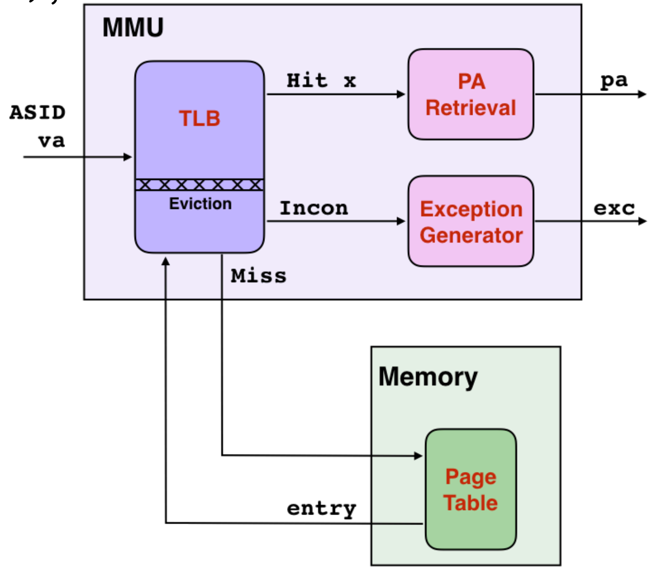

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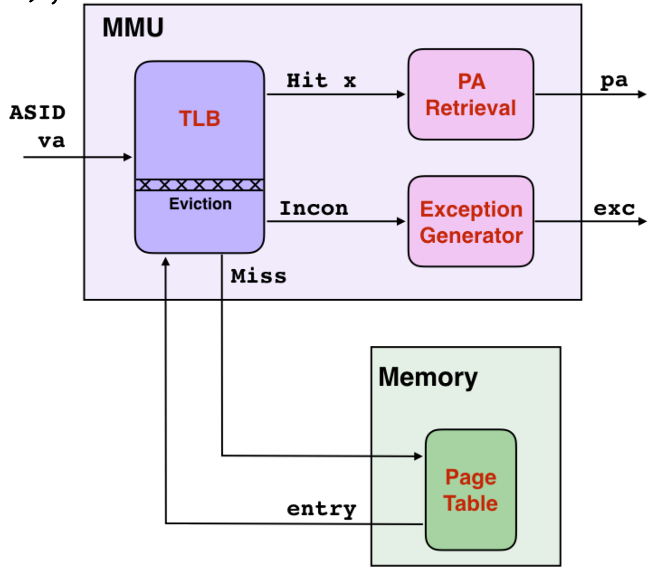

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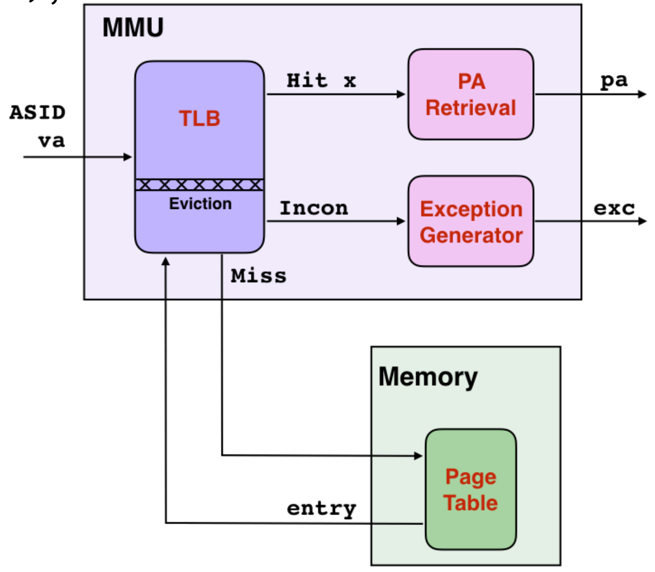

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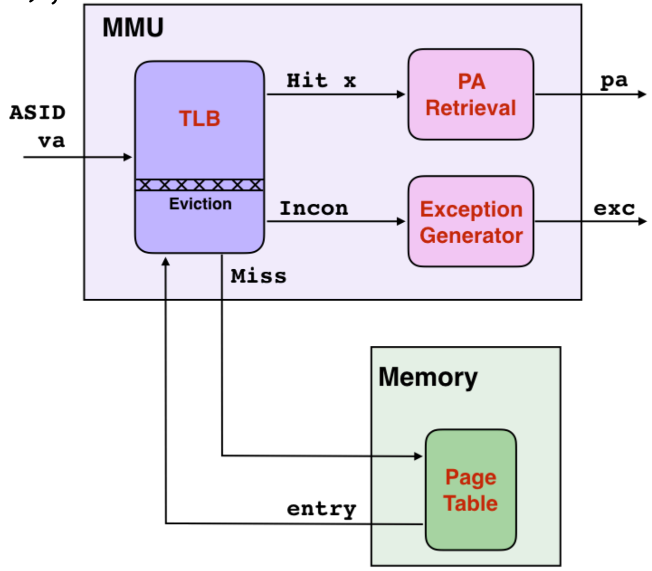

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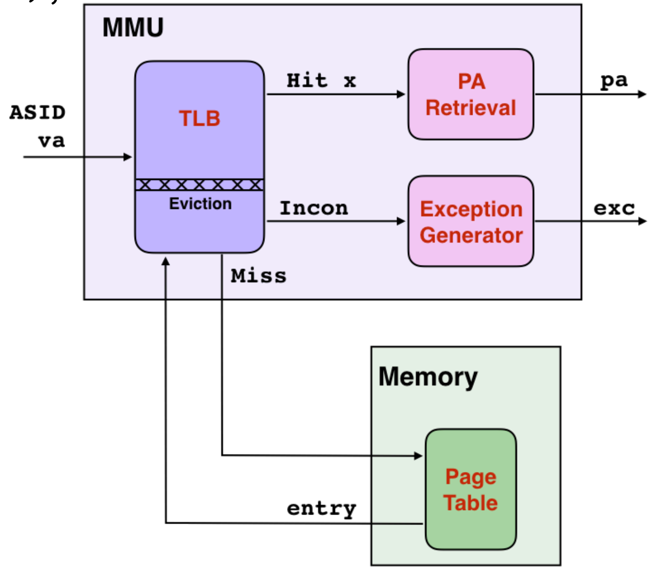

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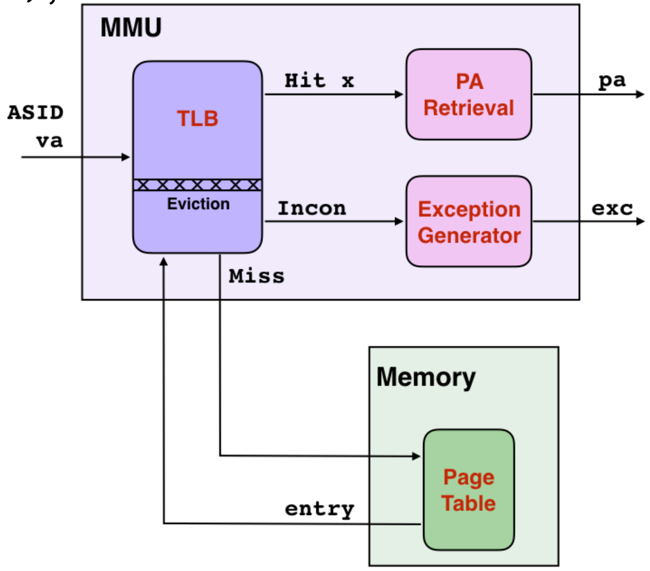

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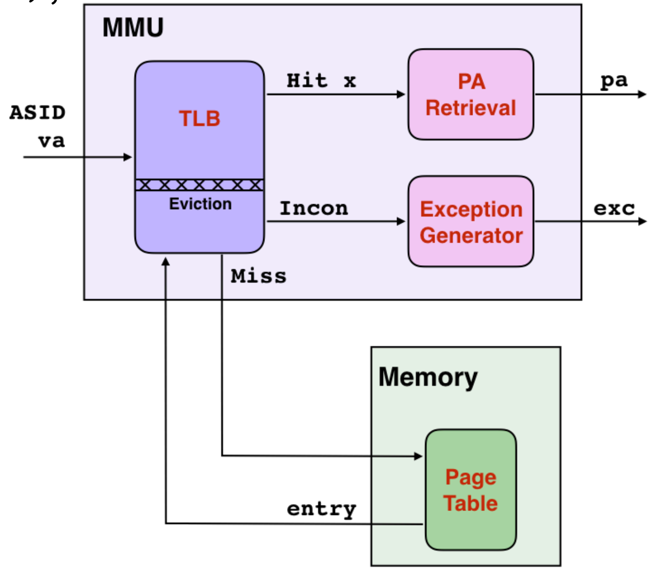

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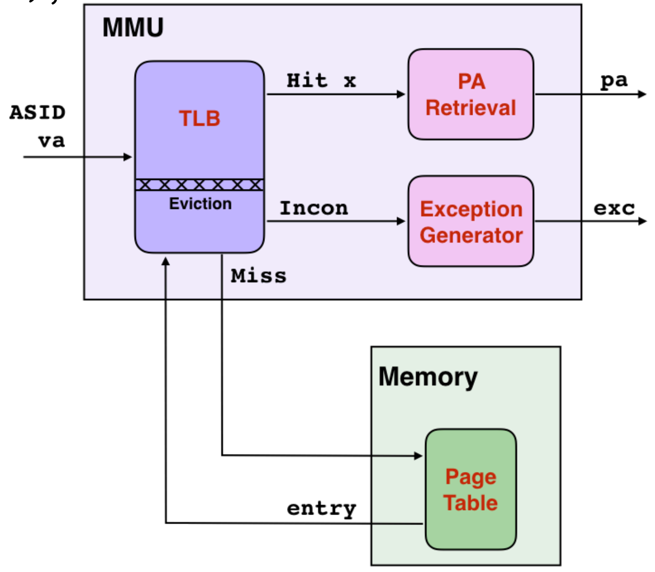

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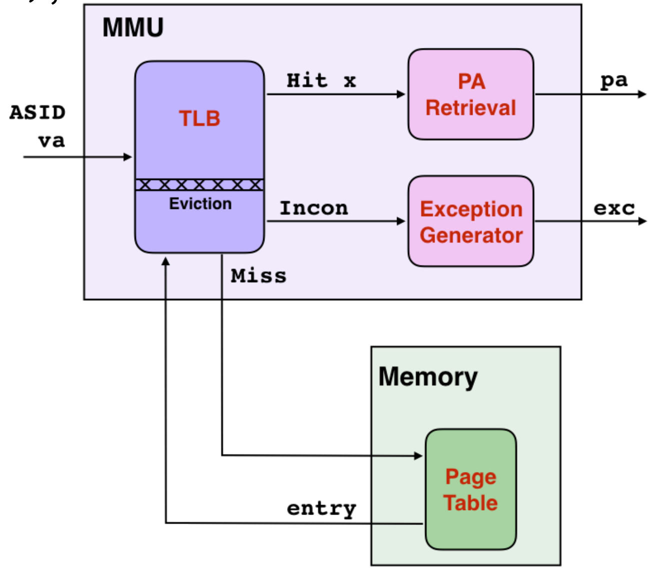

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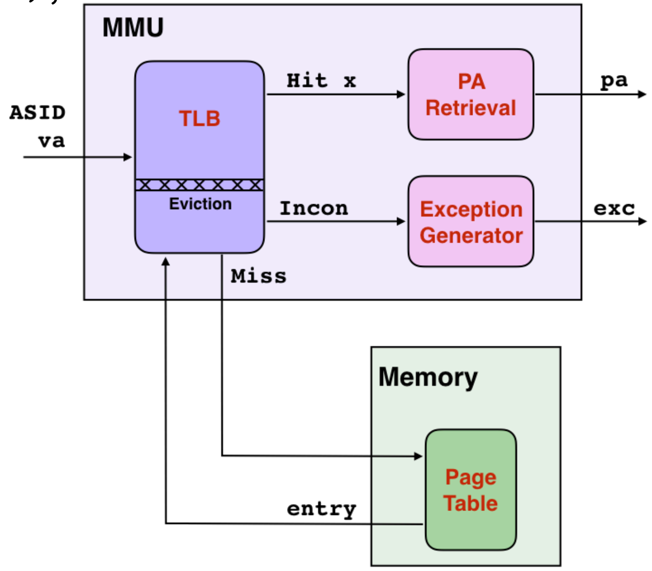

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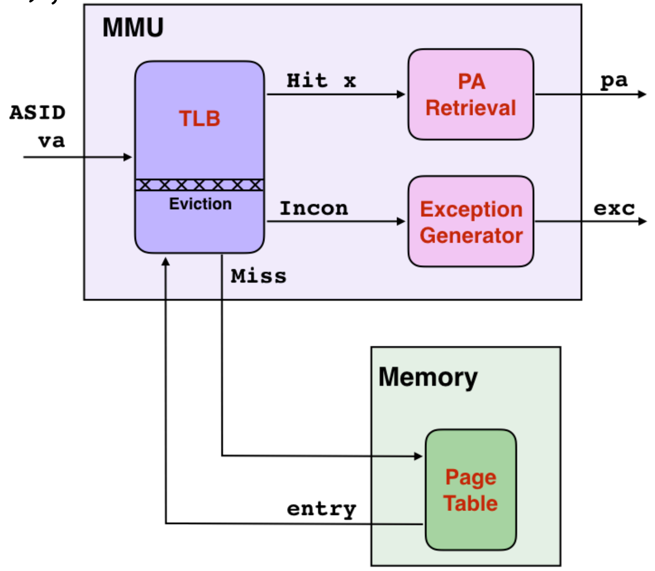

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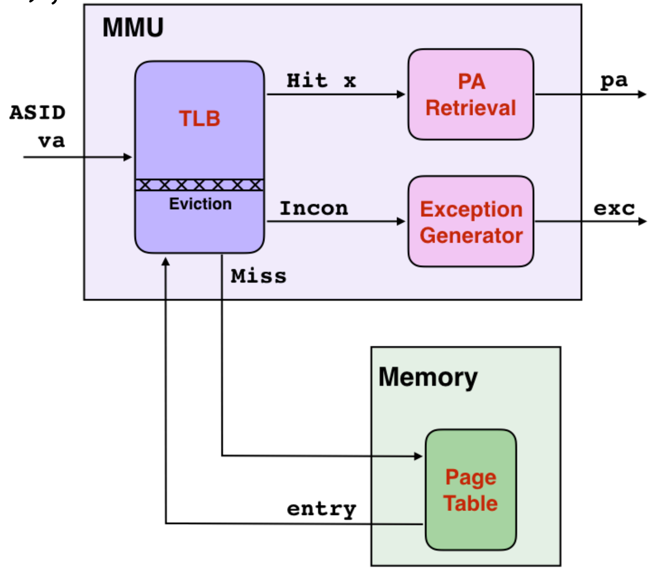

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mmu_write (val, va, sz) = do {
  pa ← mmu_translate va;
  mem_write (val, pa, sz)
}
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mmu_read (va, sz) = do {
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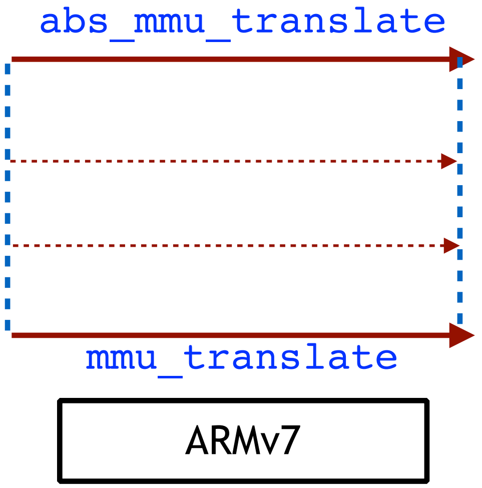
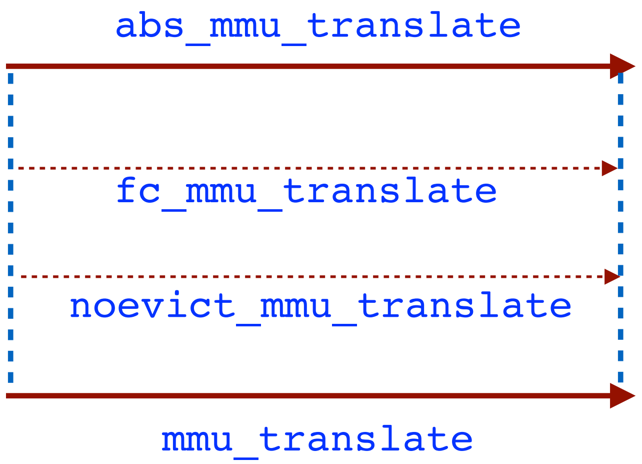


MMU Abstraction

- Stepwise data refinement for
    - abstracting eviction
    - state invariance in case of
        - memory read
        - memory write outside of page tables
    - complete abstraction for TLB



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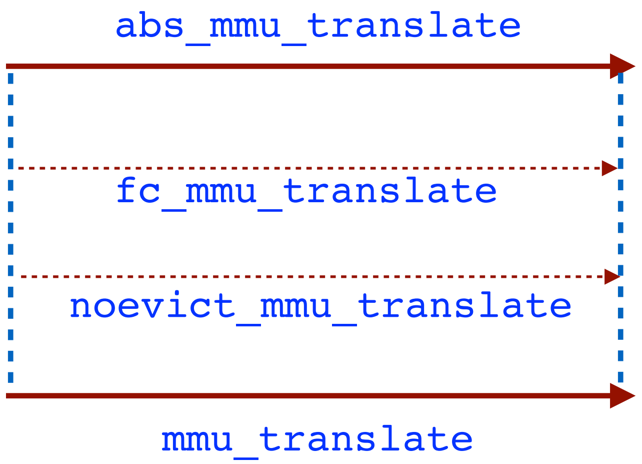

Any program that is safe with abstracted MMU
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Abstracting Eviction

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- TLB with fewer entries is always more consistent than one with more entries

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Miss < Hit < Incon
```

$\texttt{t} \subseteq \texttt{t'} \Longrightarrow \texttt{lookup t a v} \leq \texttt{lookup t' a v}$

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t ⊆ t’ ⟹ lookup t a v ≤ lookup t’ a v

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  - identical to `mmu_translate` except it doesn’t evict entries

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$$\begin{tikzcd}
\mathbf{t} \arrow[r, "\texttt{noevict\_mmu\_translate va}"] \arrow[d, dotted, no head, "\texttt{TLB } s \subseteq \texttt{TLB } t"'] & \mathbf{t'} \arrow[d, dotted, no head, "\texttt{TLB } s' \subseteq \texttt{TLB } t'"] \\
\mathbf{s} \arrow[r, "\texttt{mmu\_translate va}"'] & \mathbf{s'}
\end{tikzcd}$$

`invariant: consistent w.r.t va`

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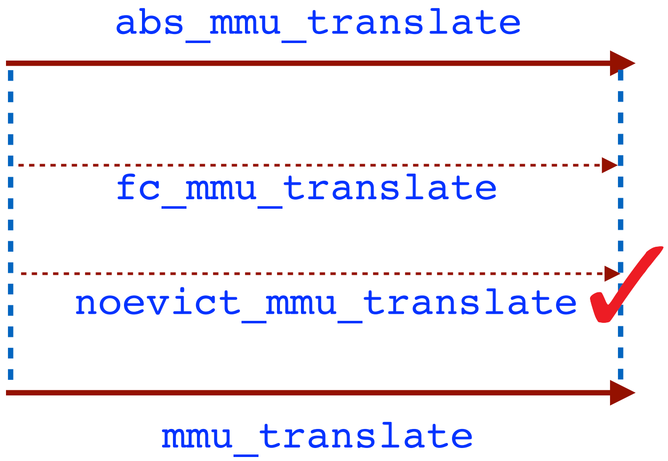

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State Invariance

- `fc_mmu_translate`
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State Invariance - Memory Access

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- Memory read

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  - user-level programs
  - seL4 static address mappings

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    - memory read ✓
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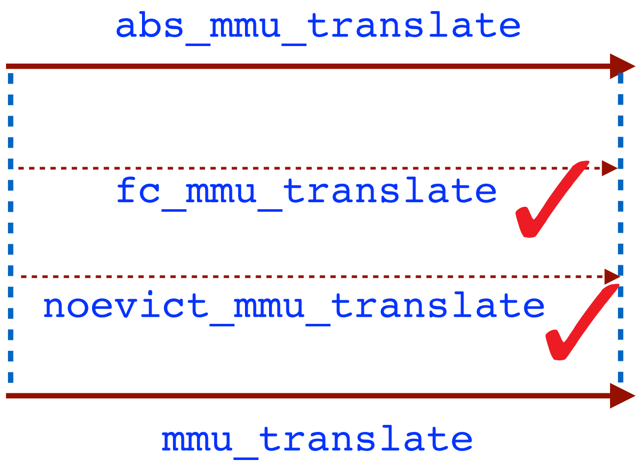

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$$\begin{tikzcd}
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invariant: va ∉ incon_set t

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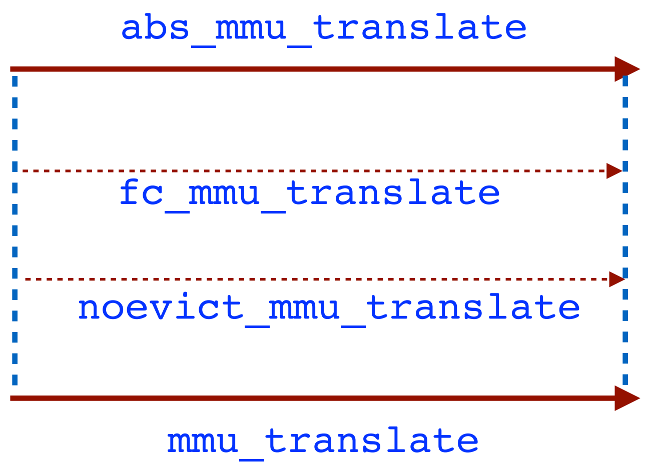
No state change at all, apart from potentially raising exceptions

`invariant: va ∉ incon_set t`

Taken Together

- TLB should be transparent to programs if maintained correctly

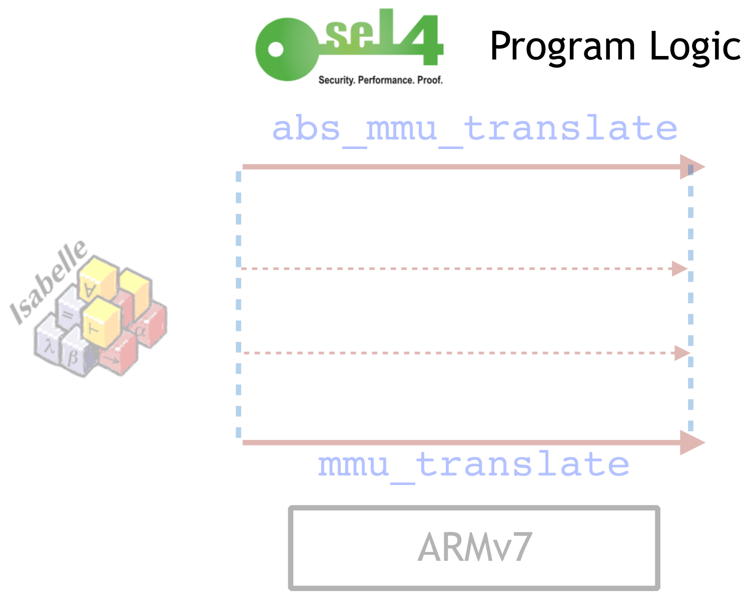
- Refinement chain



- Cached page table walks in ARMv7-A

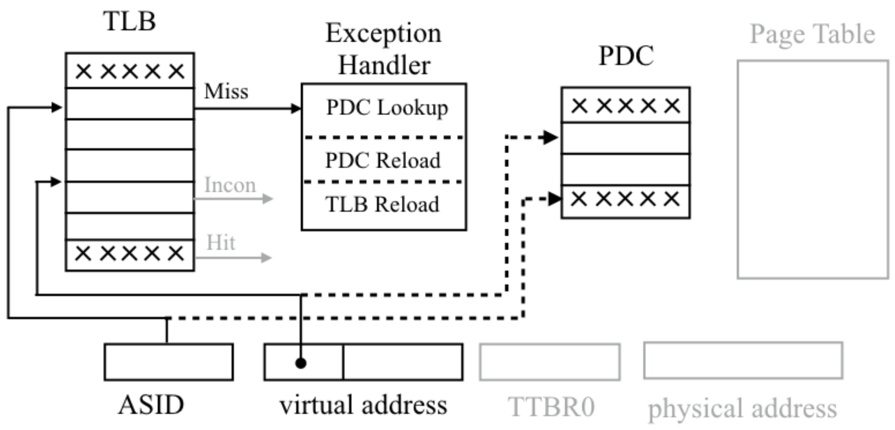
- Abstraction
  - hides low-level hardware TLB details
  - easy to reason about
  - reduction theorems

Future Direction



Thank You

Caching Partial Walks



Caching Partial Walks

- Hardware caching of partial page table walks
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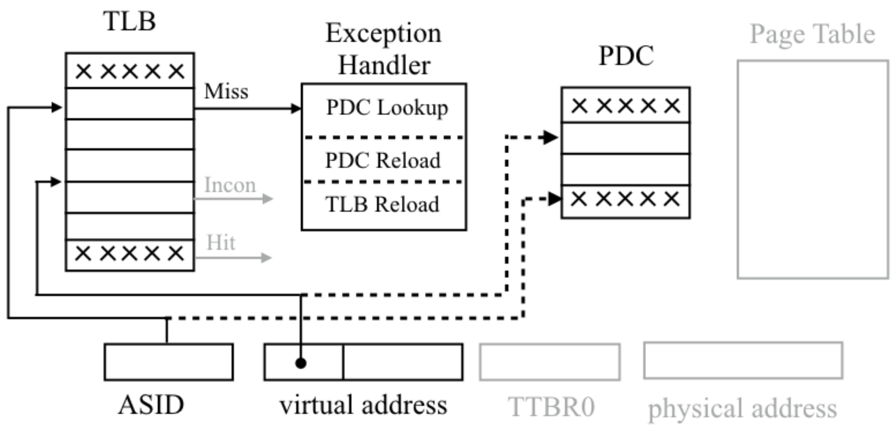

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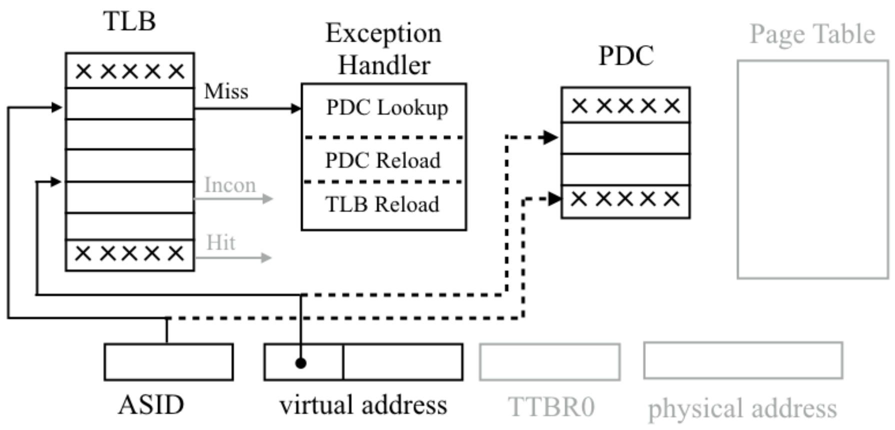

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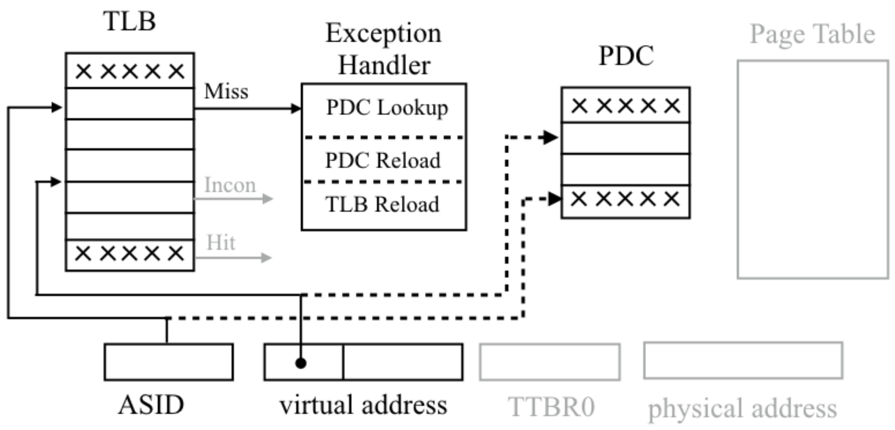

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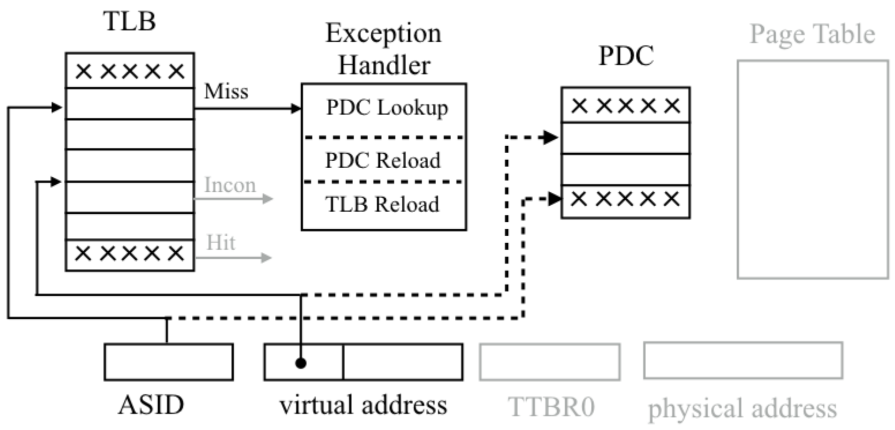

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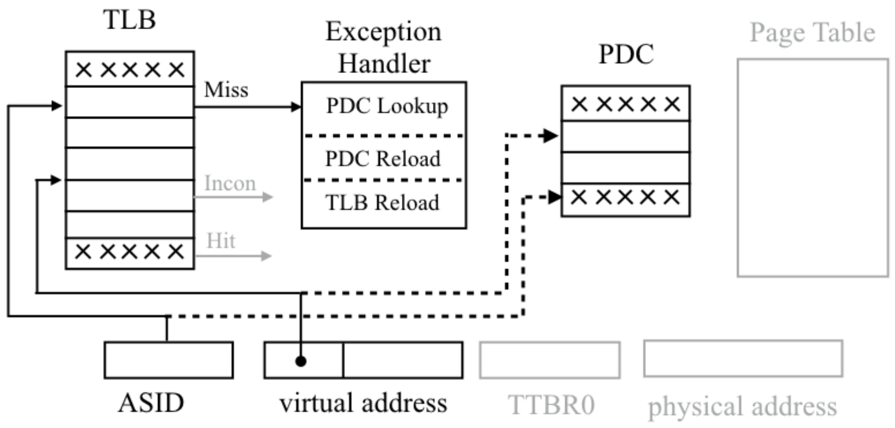
  - concrete, saturated



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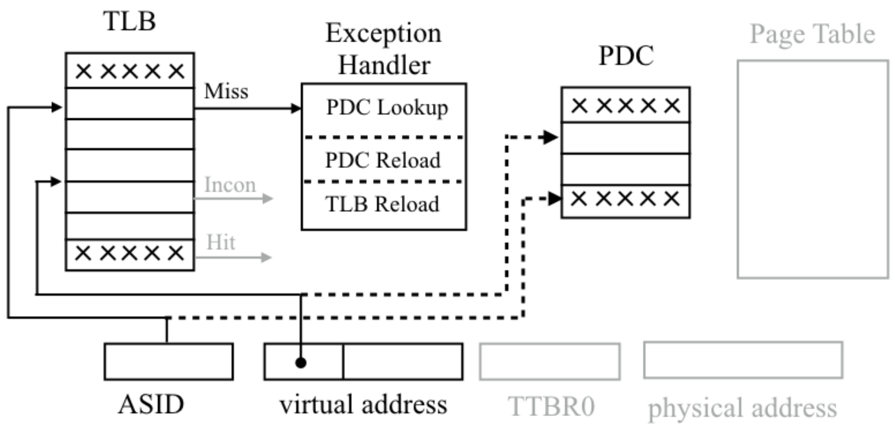

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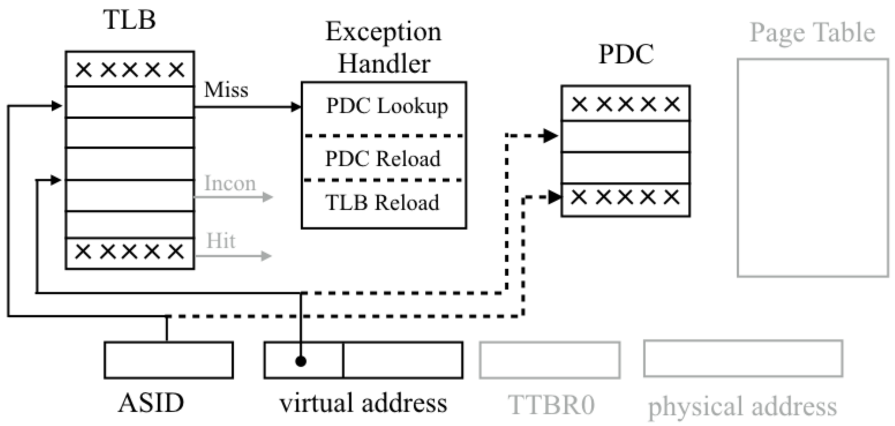

- Saturation
  - Cache hierarchy
  - Step-wise refinement to fully abstract PDC and TLB