Program Verification in the Presence of Cached Address Translation

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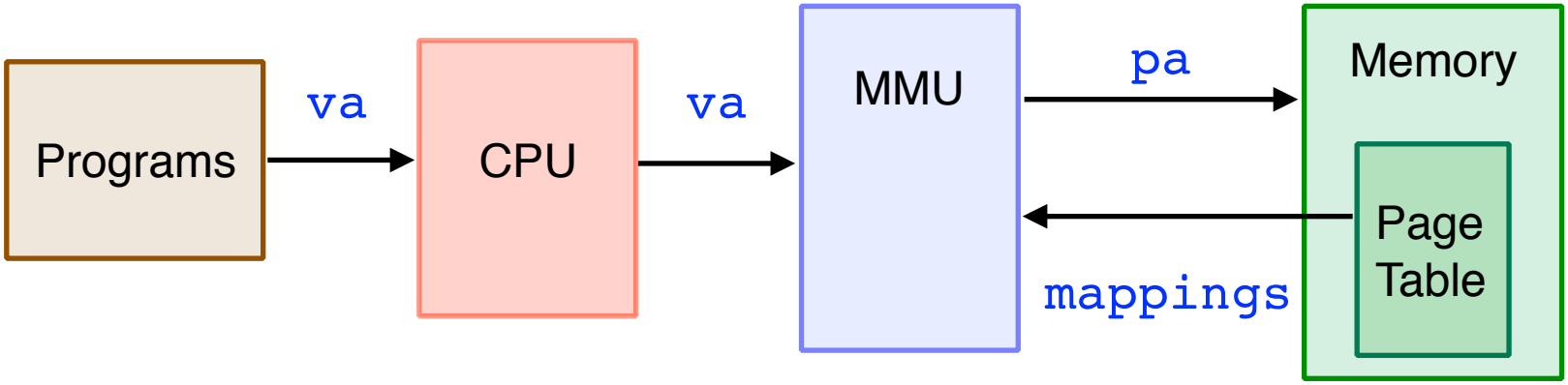
What is
Cached Address Translation



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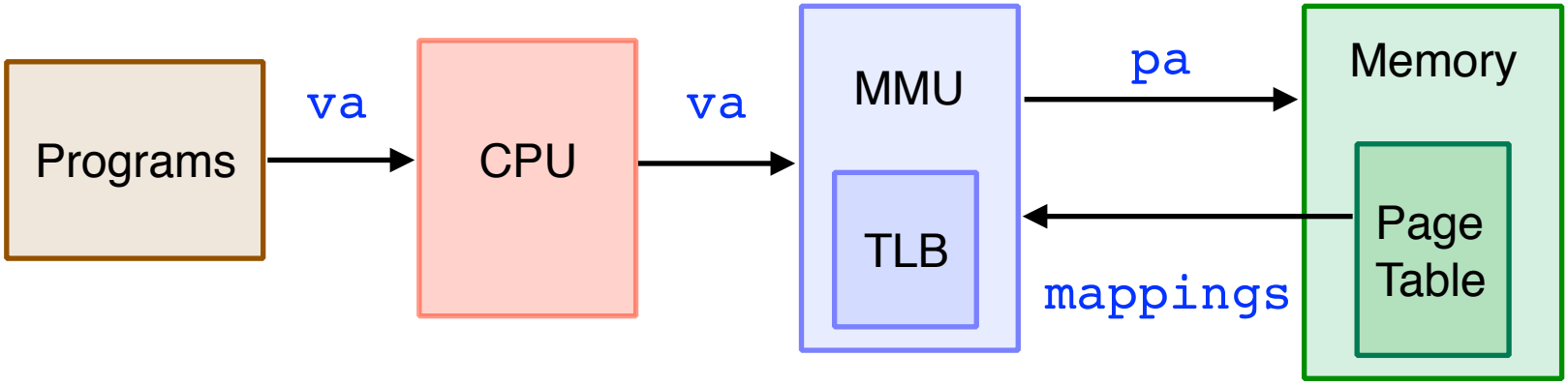

- Translation Lookaside Buffer (TLB) is
  - a dedicated cache for page table walks
  - architecture specific
  - managed by hardware and operating system together

TLB Effects on Program Execution

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- TLB being cache
  - has *no* functional effects
  - only makes execution faster, *if* maintained correctly
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- TLB-aware logic for program reasoning
  - abstract model for ARMv7-style MMU

Contributions

- TLB-aware program logic in Isabelle/HOL
  - sound abstraction of ARMv7-style MMU
  - language with TLB management primitives
  - TLB-aware Hoare logic rules

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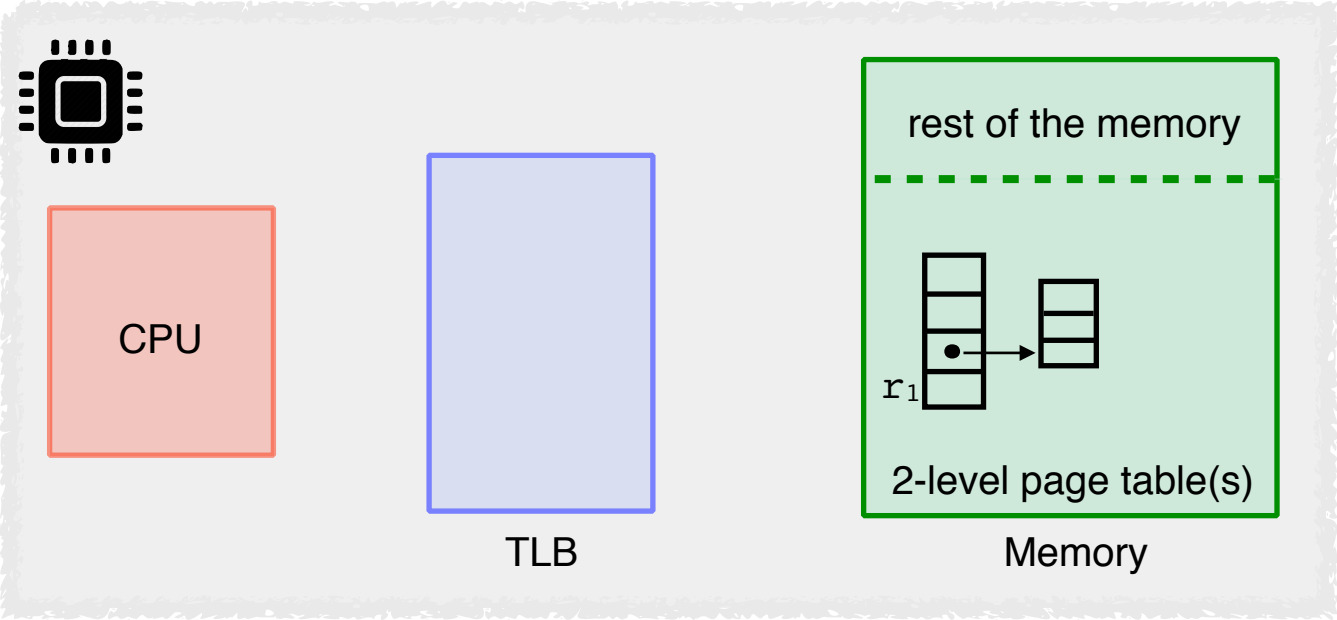
ARMv7-style MMU



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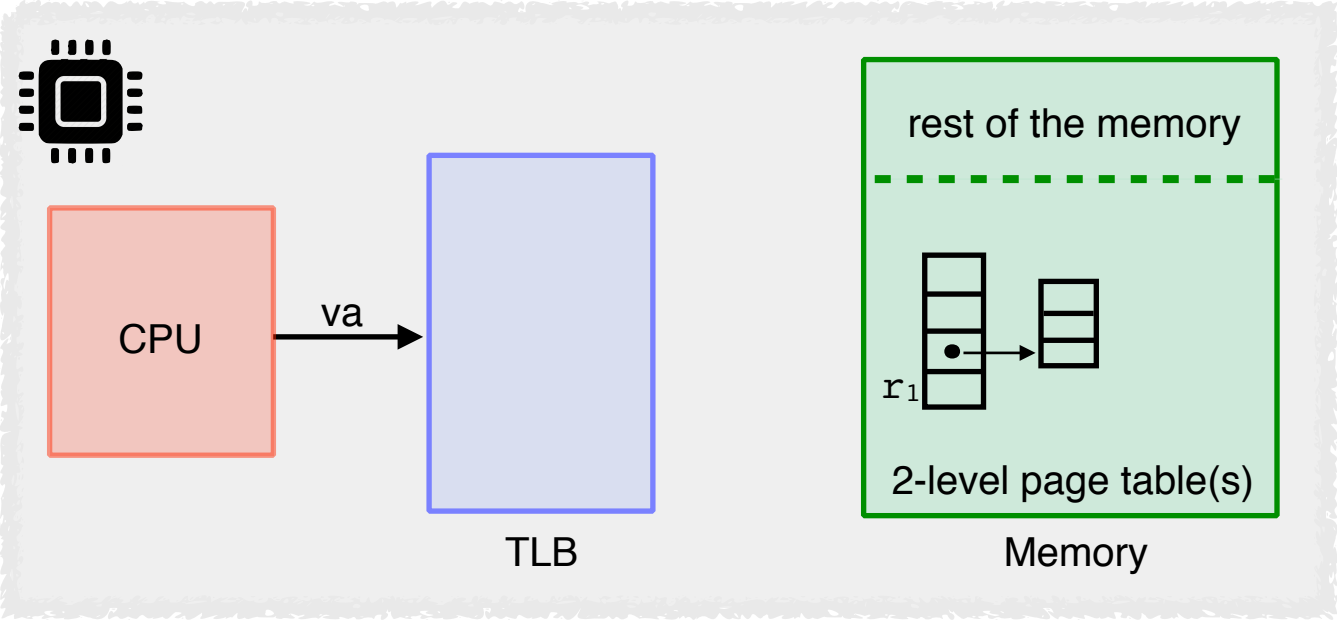

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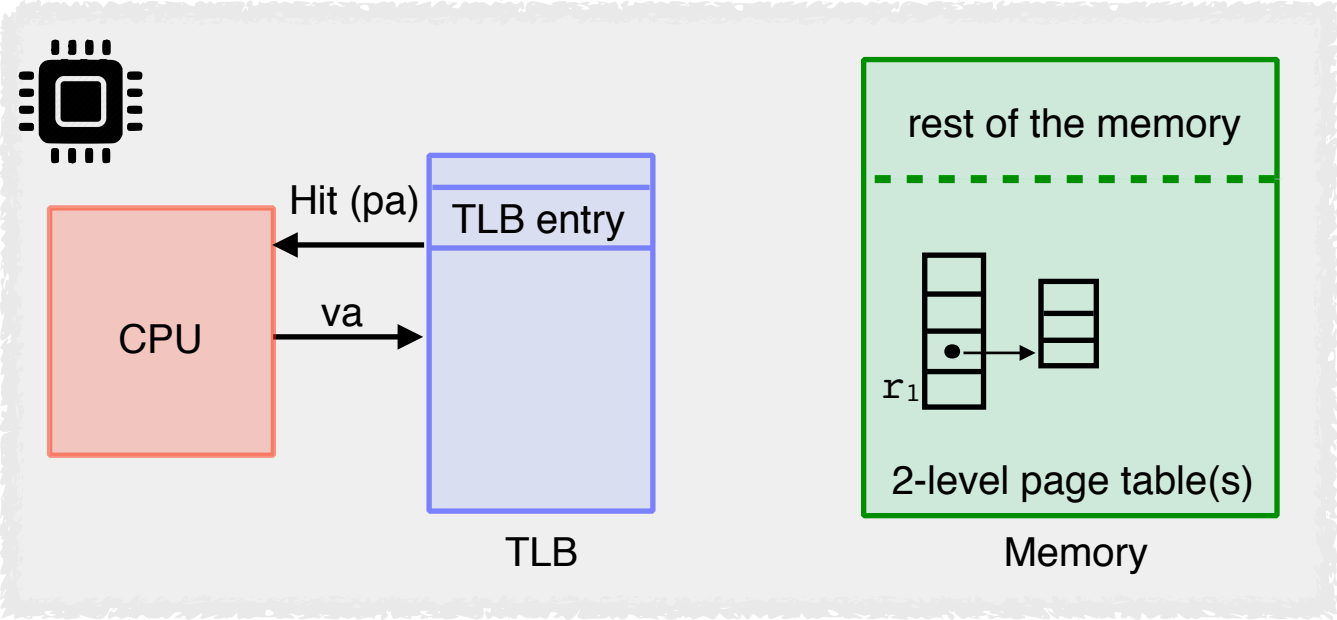

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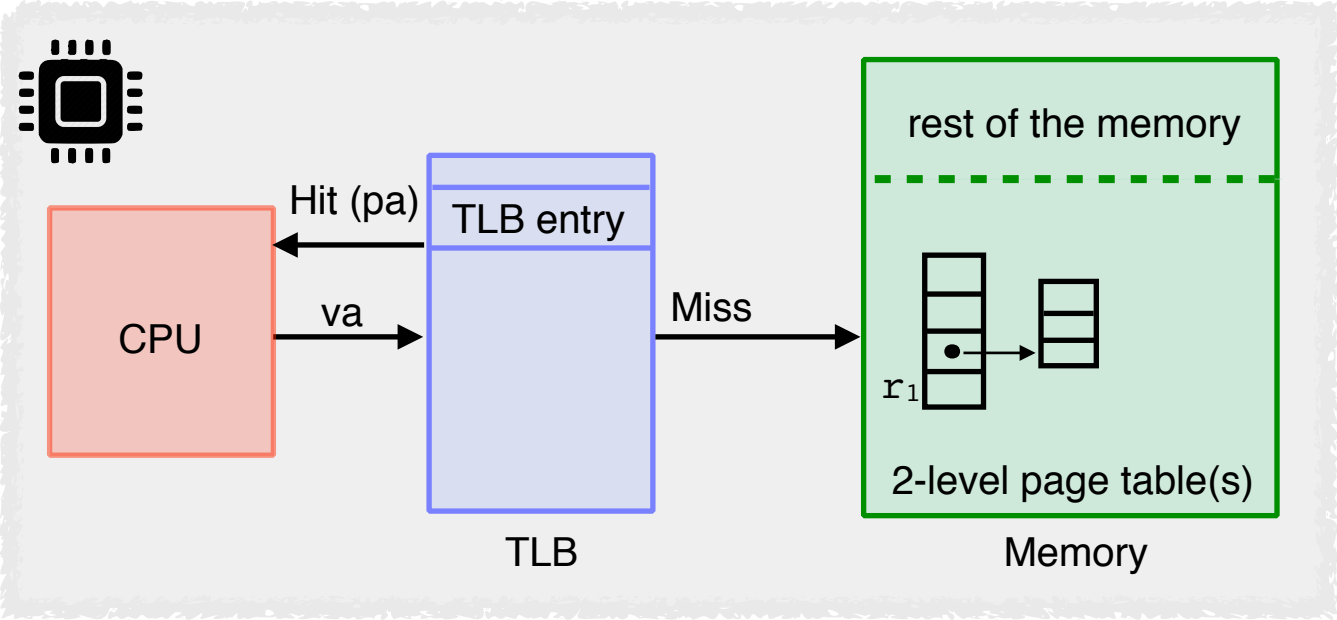

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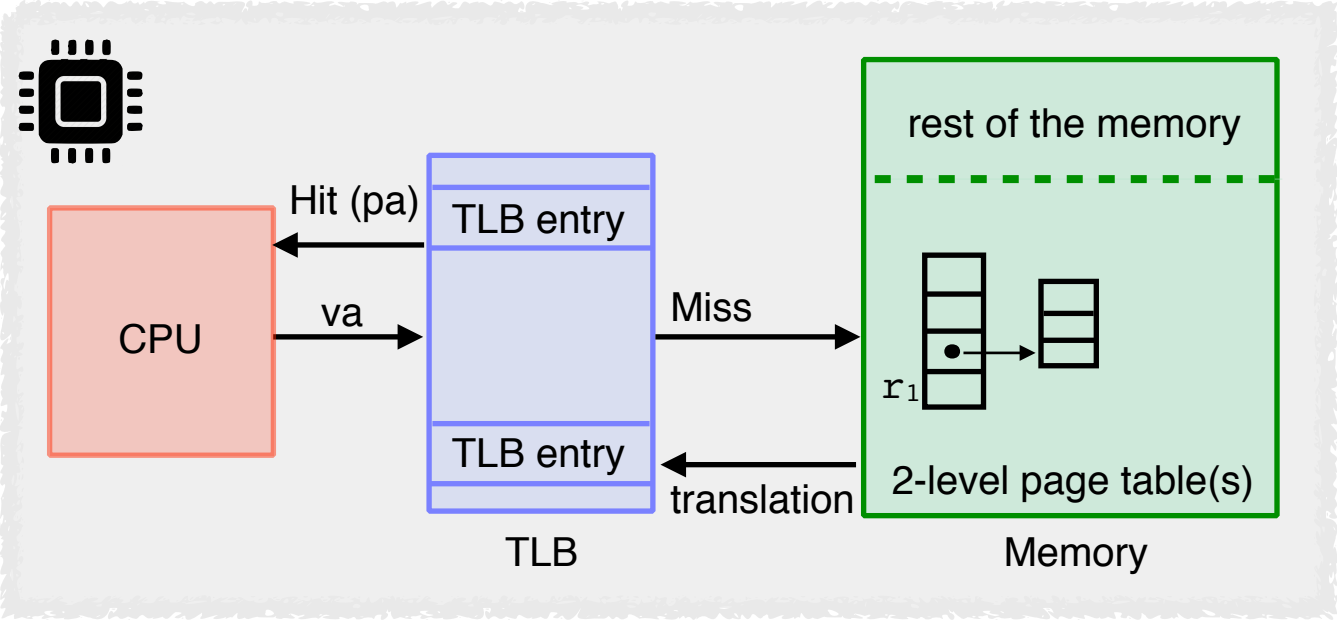

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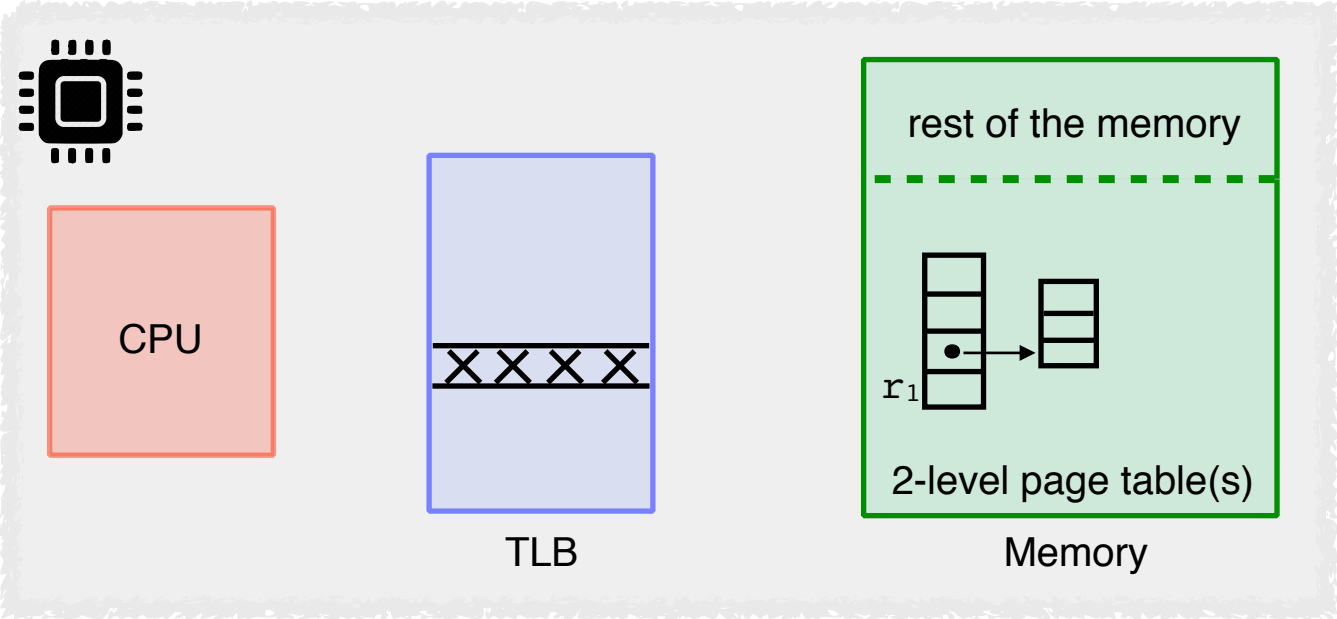
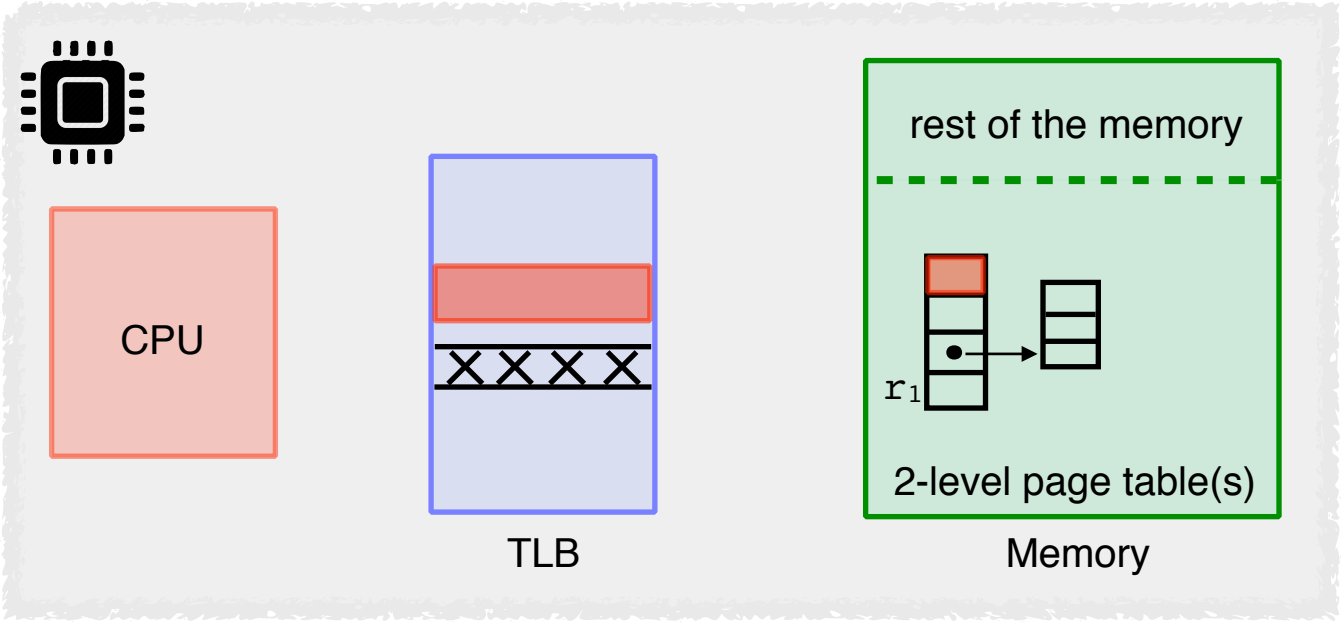


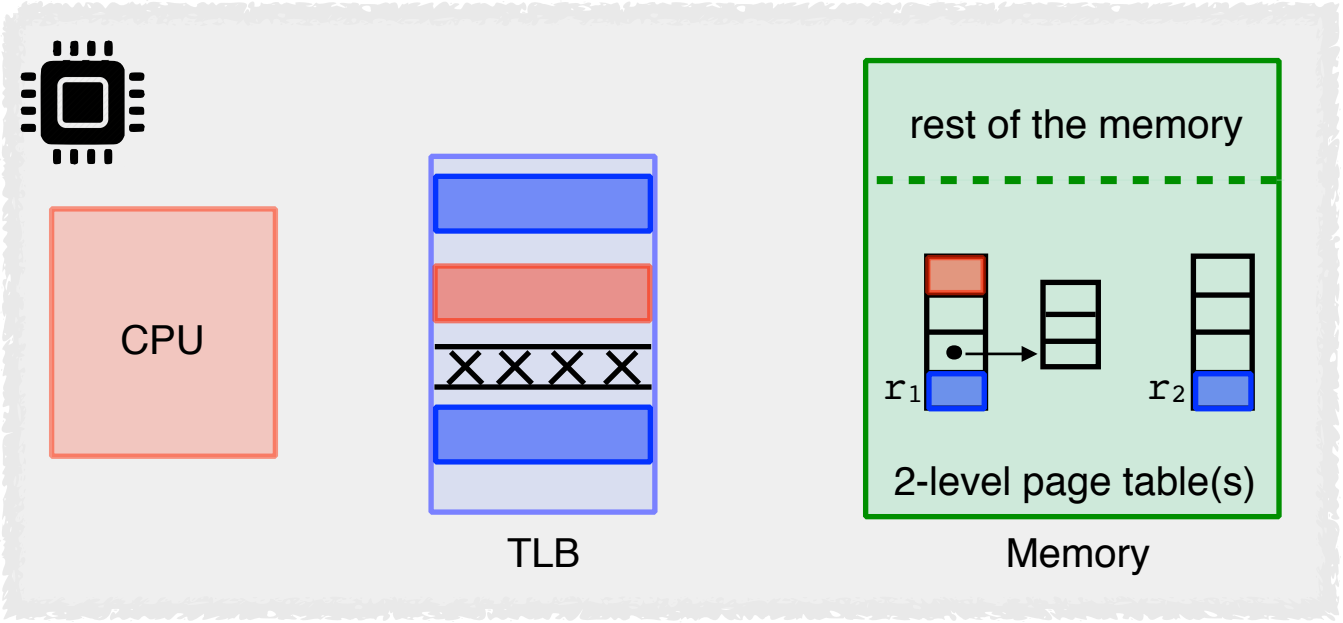
- TLB eviction (××)

ARMv7-style MMU



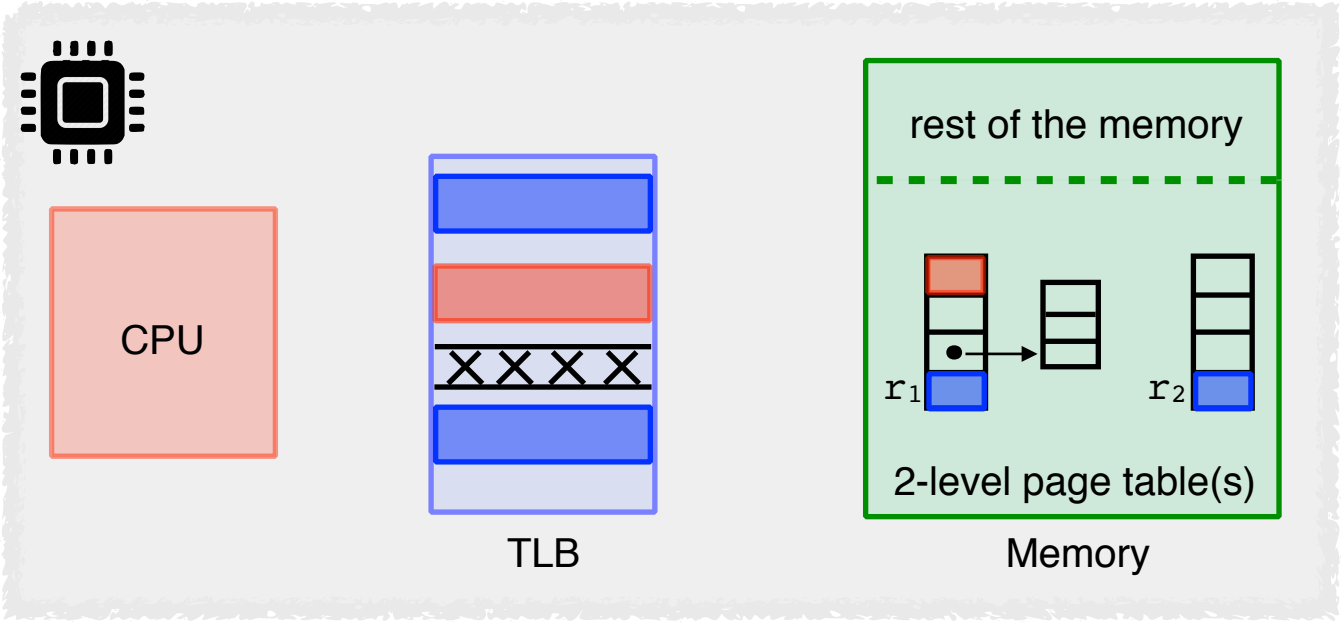
- TLB eviction (✕✕)
- TLB incoherency (▭)
  - stale translation entries w.r.t. page table(s)

ARMv7-style MMU



- TLB eviction (✕✕)
- TLB incoherency (▭)
  - stale translation entries w.r.t. page table(s)
- TLB inconsistency (▭)
  - more than one translation entries

ARMv7-style MMU



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  - page table(s)
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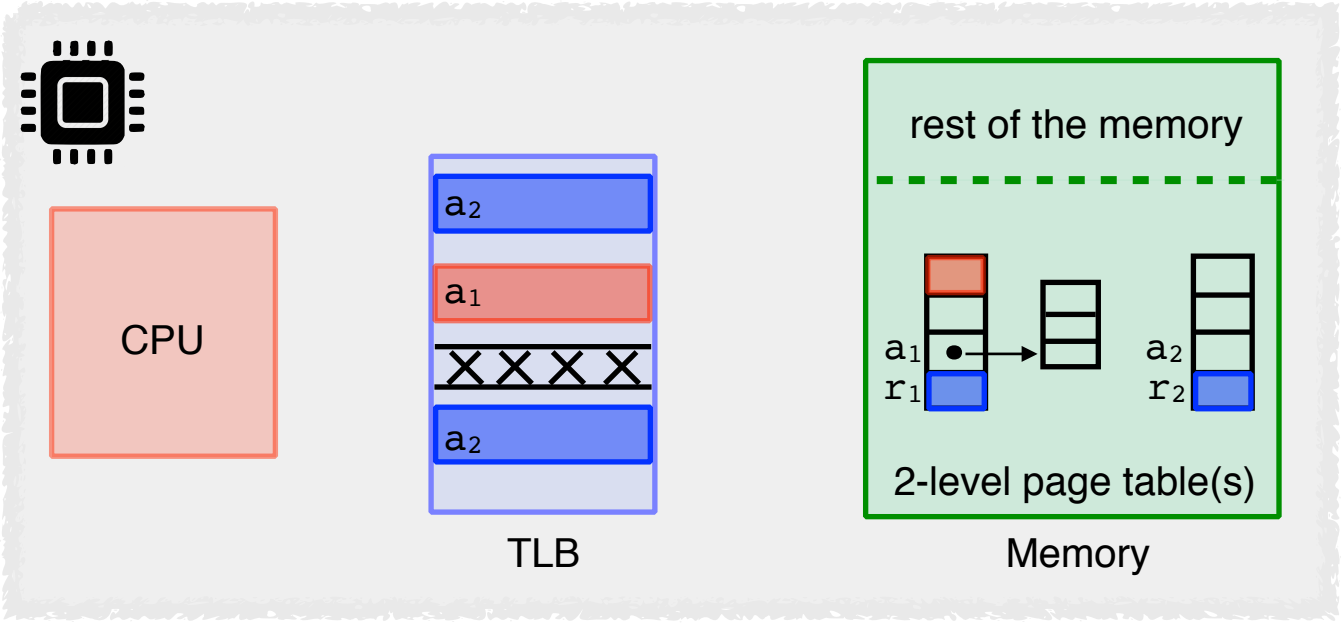

- TLB maintenance operations after updating
  - page table(s)
  - root register
- Selective invalidation using Address Space IDentifier - ASID
  - ASID register

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  - hardware details
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Stepwise data refinement
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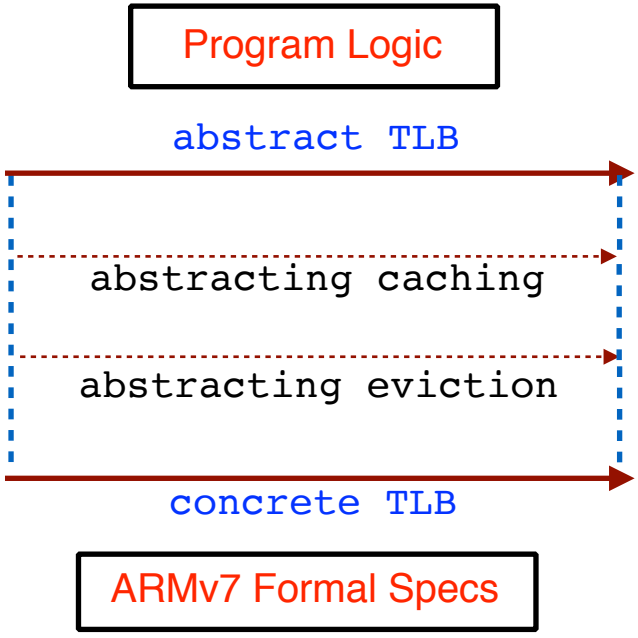

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Stepwise data refinement
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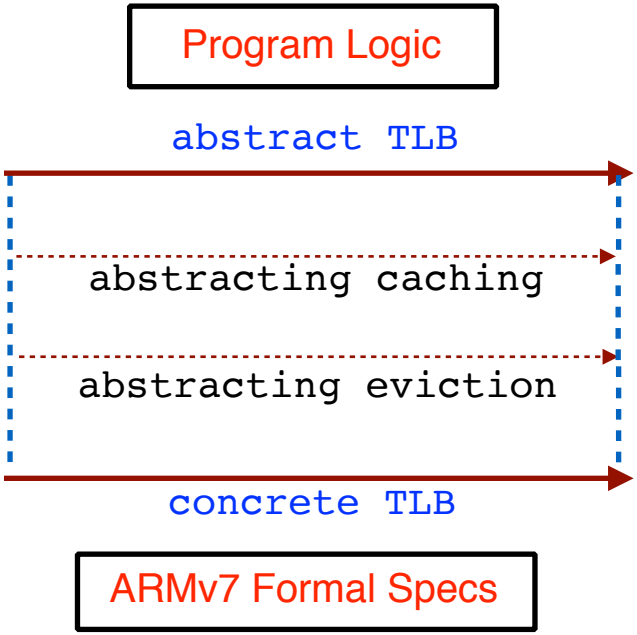
Functionality of a TLB
is captured by the record of
inconsistent virtual addresses

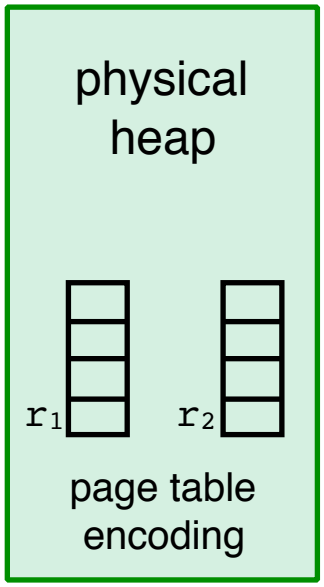


Sound Abstraction of ARMv7-style MMU

processor mode

active ASID

active root



abstract TLB

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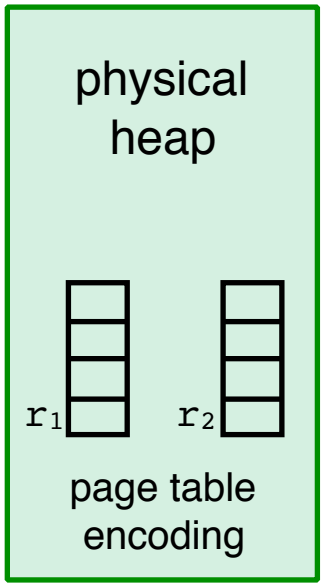

abstract TLB

incon_set	pt_snapshot
set of inconsistent vaddrs for active ASID	page table state for all inactive ASIDs

Sound Abstraction of ARMv7-style MMU

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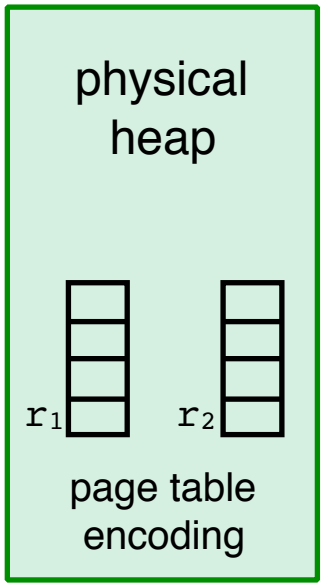

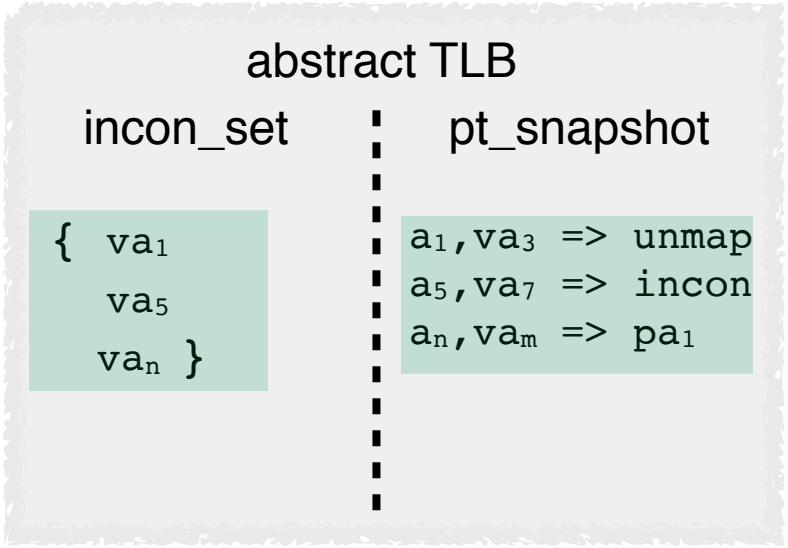

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- Heap language with TLB management primitives
  - arithmetic expressions **`aexp`**
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  - boolean expressions **`bexp`**
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      - `flushALL`, `flushASID`, `flushVA` and `flushASIDVA`
    - updateRoot
    - updateASID
    - updateMode
      - `kernel` or `user`

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Program Logic

- Operational semantics
  - **`aexp`** — partial function from **`state`** to 32-bit **`value`**
  - **`bexp`** — partial function from **`state`** to **`bool`**
  - **`command`** — relation between **`state`** and **`state option`**

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- Hoare triple — $\{\!|P|\!\}\ c\ \{\!|Q|\!\}$
  - soundness is derived directly from the operational semantics
  - logic rules are in weakest-precondition form

Program Logic — Rules

- assignment
- updateRoot
- updateASID

☆ other rules are in standard Hoare logic form

Program Logic — Rules

- assignment

$$\models \{\!|\lambda \mathtt{s}.\ [\![\mathtt{l}]\!]\ \mathtt{s} = \lfloor \mathtt{vp} \rfloor \wedge [\![\mathtt{r}]\!]\ \mathtt{s} = \lfloor \mathtt{v} \rfloor \wedge \mathtt{vp} \notin \mathcal{IC}\ \mathtt{s} \wedge \mathtt{Addr\ vp} \hookrightarrow_s \mathtt{pp} \wedge \mathtt{P\ (heap\_iset\_update}_s\ \mathtt{(pp} \mapsto \mathtt{v))}|\!\}$$
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comparison of the active page table
before and after the assignment for
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before assignment	after assignment
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`va3 is mapped to pa3`	
`va4 is mapped to pa4`	

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`va4 is mapped to pa4`	`va4 is unmapped`

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Program Logic — Rules

- assignment ✓
- updateRoot
- updateASID

Program Logic — Rules

- updateRoot

$$\models \{\!|\lambda s.\ \texttt{kernel s} \wedge [\![\texttt{rte}]\!]\ \texttt{s} = \lfloor \texttt{rt} \rfloor \wedge \texttt{P (root\_iset\_update}_s\ \texttt{Addr rt)}|\!\}$$
$$\texttt{updateRoot rte}\ \{\!|\texttt{P}|\!\}$$

✓ available in kernel mode

✓ reasoning about `root` and `incon_set` update

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`incon_set` update:

comparison of the two page tables
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Steps:

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Steps:

1

store the `incon_set` and the page table of the active ASID to the `pt_snapshot`

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Steps:

1 store the `incon_set` and the page table of the active ASID to the `pt_snapshot`

2 update the ASID

Program Logic — Rules

- updateASID

$\{\lambda s.\ \texttt{kernel s} \wedge \texttt{P (asid\_pt\_snpshot\_update}_s\ \texttt{a)}\}\ \texttt{updateASID a}\ \{\texttt{P}\}$

Steps:

1 store the `incon_set` and the page table of the active ASID to the `pt_snapshot`

2 update the ASID

3 compute new `incon_set` from the `pt_snapshot` and the active page table

Program Logic — Rules

- updateASID

$\{\!|\lambda s.\ \texttt{kernel s} \wedge \texttt{P (asid\_pt\_snpshot\_update}_s\ \texttt{a)}|\!\}\ \texttt{updateASID a}\ \{\!|\texttt{P}|\!\}$

Steps: switching from a_1 to a_2

before updateASID	after updateASID
active_ASID : a_1	active_ASID :
incon_set : { va_3 , va_7 }	incon_set : { , }
pt_sanpshot: a_1, va_3 => unmap a_1, va_7 => pa_1 a_1, va_6 => unmap a_2, va_1 => Incon a_2, va_6 => pa_2	pt_snapshot:
page table: va_6 => pa_7	

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Steps: switching from a_1 to a_2

before updateASID

active_ASID : a_1

incon_set : { va_3 , va_7 }

pt_sanpshot:
a_1, va_3 => unmap
a_1, va_7 => pa_1
a_1, va_6 => unmap
a_2, va_1 => Incon
a_2, va_6 => pa_2

page table: va_6 => pa_7

after updateASID

active_ASID :

incon_set : { , }

pt_snapshot:
a_1, va_3 => Incon
a_1, va_7 => Incon
a_1, va_6 => pa_7

1

Program Logic — Rules

- updateASID

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active_ASID : a_1

incon_set : { va_3 , va_7 }

pt_sanpshot:
a_1, va_3 => unmap
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a_1, va_6 => unmap
a_2, va_1 => Incon
a_2, va_6 => pa_2

page table: va_6 => pa_7

after updateASID

active_ASID : a_2 **2**

incon_set : { , }

pt_snapshot:
a_1, va_3 => Incon
a_1, va_7 => Incon
a_1, va_6 => pa_7

Program Logic — Rules

- updateASID

$\{\lambda s.\ \text{kernel } s \wedge P\ (\text{asid\_pt\_snpshot\_update}_s\ a)\}$ updateASID a $\{P\}$

Steps: switching from a_1 to a_2

before updateASID

active_ASID : a_1

incon_set : { va_3 , va_7 }

pt_sanpshot:
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a_1, va_6 => unmap
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page table: va_6 => pa_7

after updateASID

active_ASID : a_2

incon_set : { va_1 , va_6 } **3**

pt_snapshot:
a_1, va_3 => Incon
a_1, va_7 => Incon
a_1, va_6 => pa_7

Program Logic — Rules

- assignment ✓
- updateRoot ✓
- updateASID ✓

Take-away:

TLB has been reduced to consistency check

Inconsistency is recomputed after every instruction

Contributions

- TLB-aware program logic in Isabelle/HOL
  - sound abstraction of ARMv7-style MMU
  - language with TLB management primitives
  - TLB-aware Hoare logic rules

- Reduction theorems for program verification at
  - user- and kernel-level execution
  - context switch

Program Verification

- Address space management
  - inspired by seL4

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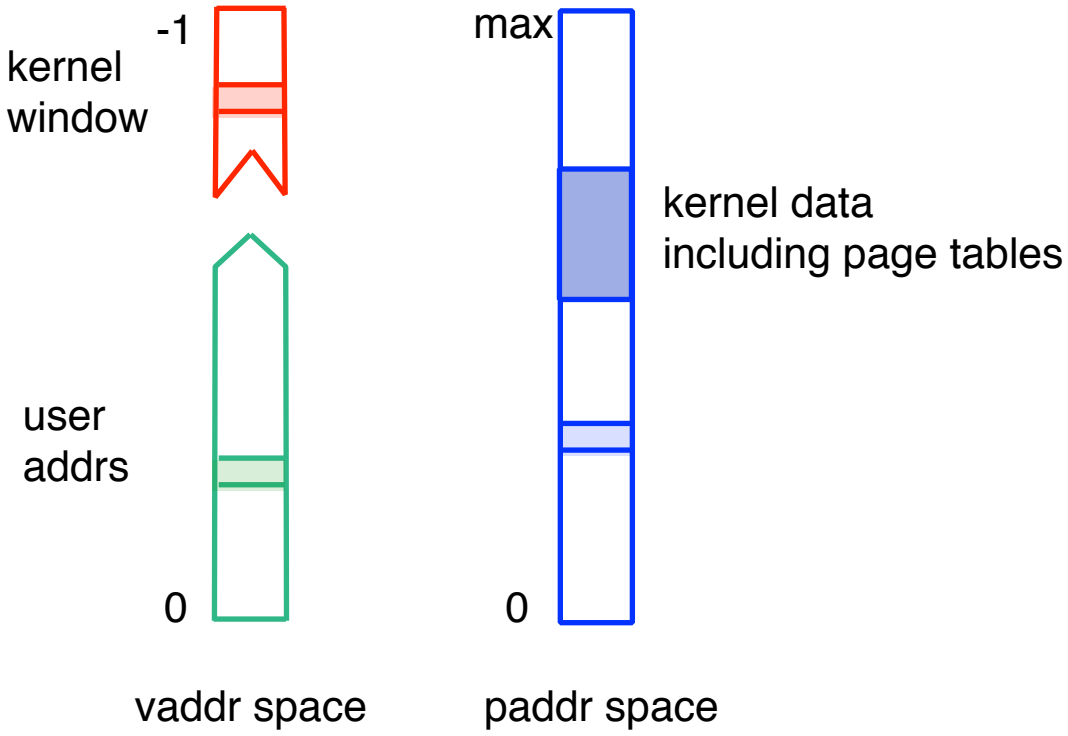

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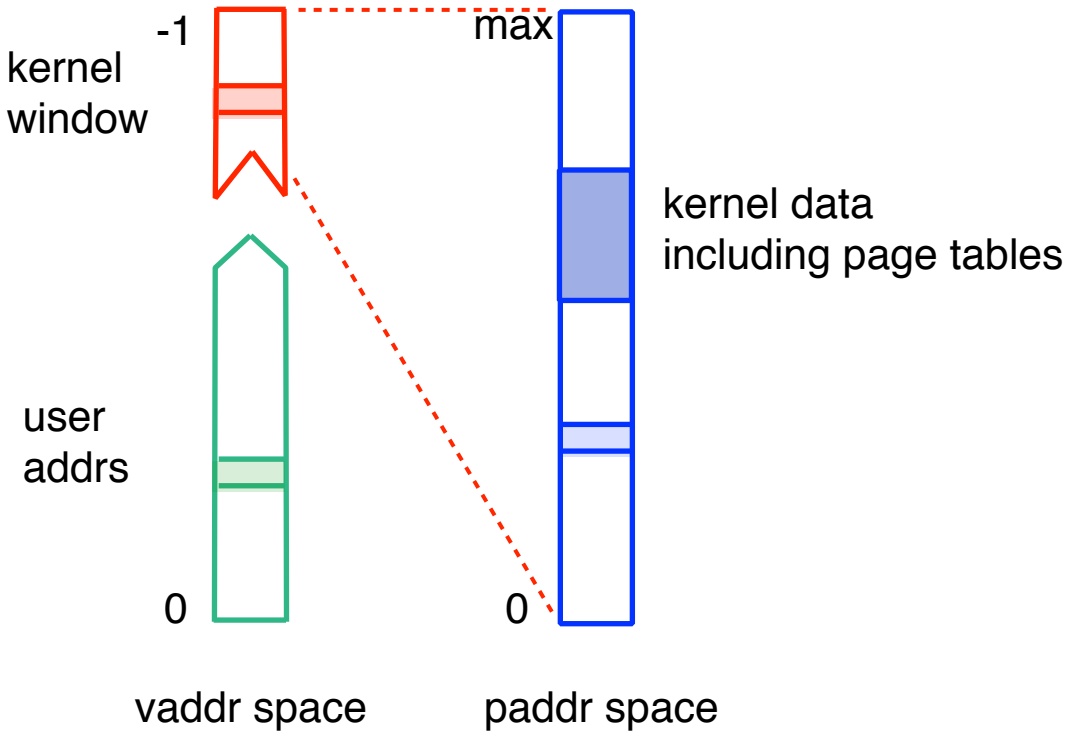

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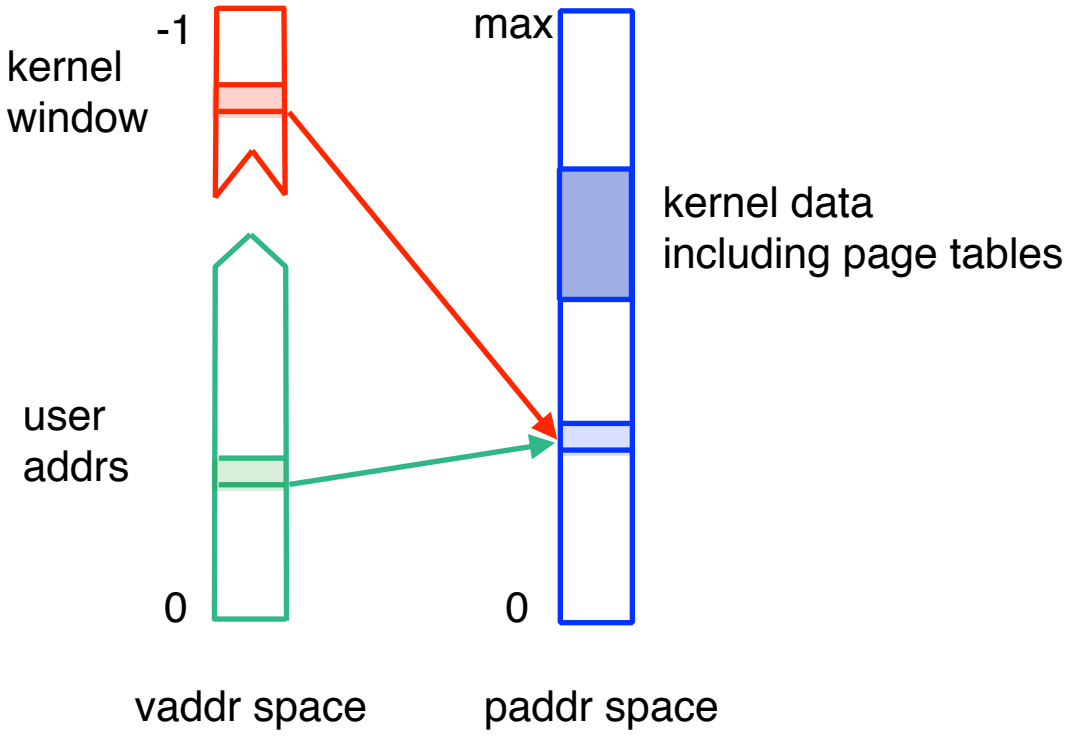

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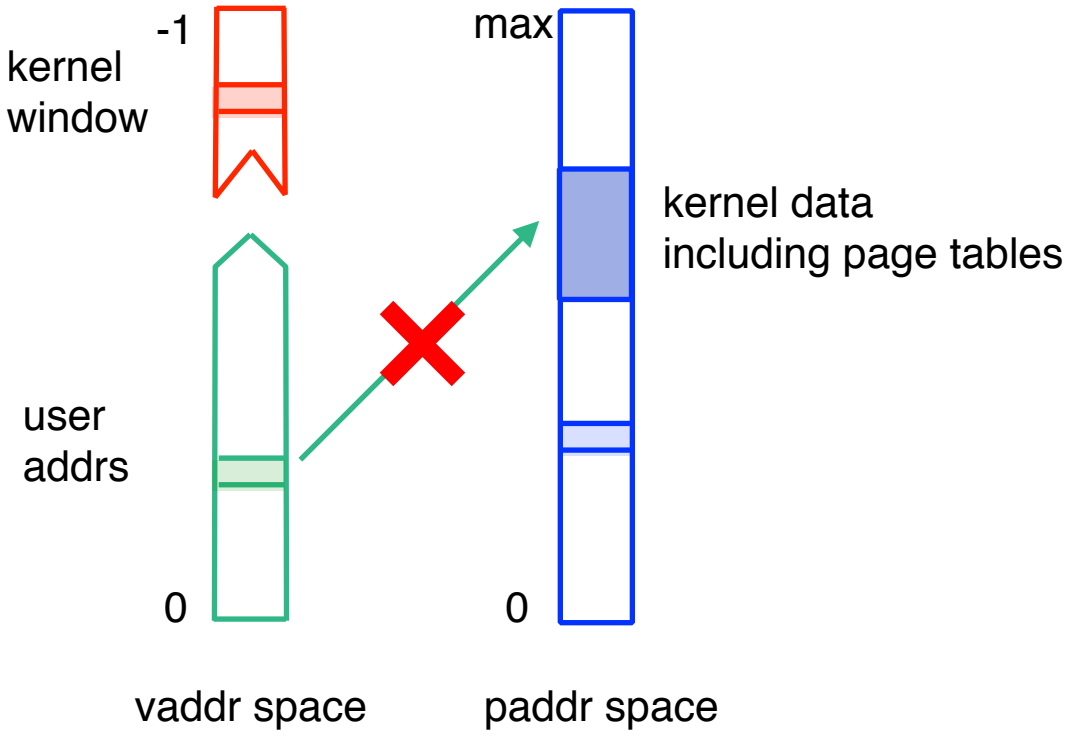

Reduction Theorems

- User-level assignment
  - user cannot update page table,
    hence cannot affect TLB consistency

$$\{\!|\lambda s.\ \texttt{mmu\_layout s} \wedge \texttt{mode s} = \texttt{User} \wedge \mathcal{IC}\ \texttt{s} = \emptyset \wedge [\![\texttt{lval}]\!]\ \texttt{s} = \lfloor \texttt{vp} \rfloor \wedge [\![\texttt{rval}]\!]\ \texttt{s} = \lfloor \texttt{v} \rfloor \wedge \texttt{Addr vp} \hookrightarrow_s \texttt{p} |\!\}$$
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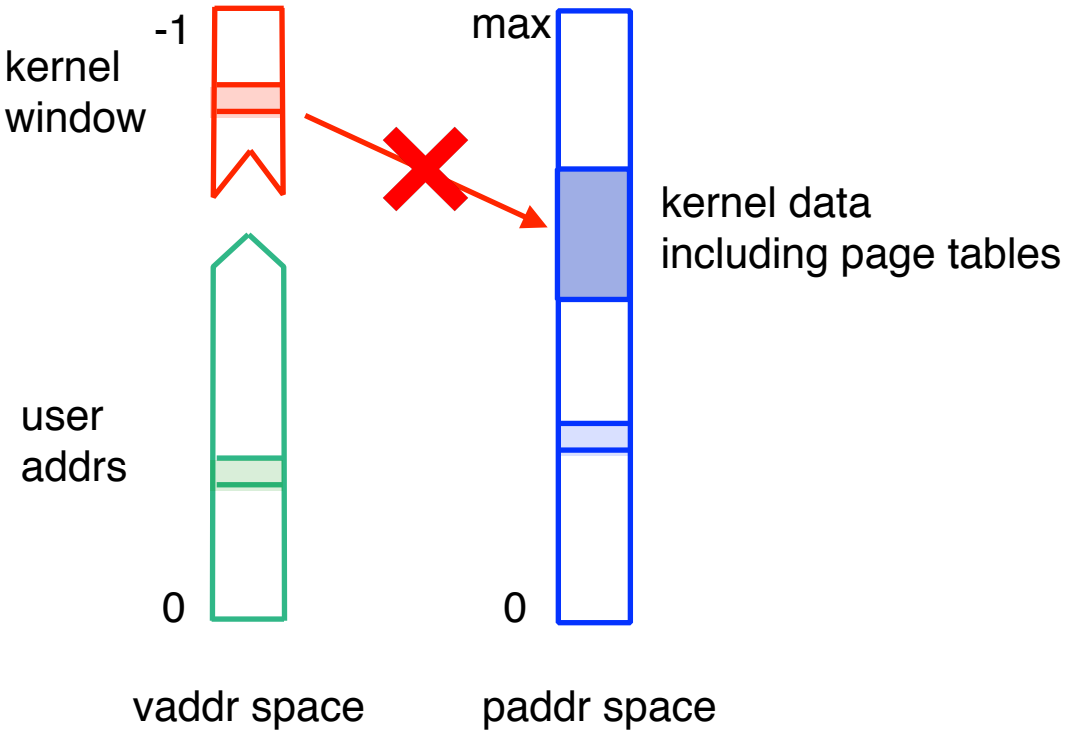
user-level reasoning has been reduced to
standard Hoare logic rule with address translation

Reduction Theorems

- Kernel-level assignment
  - that doesn't modify page table



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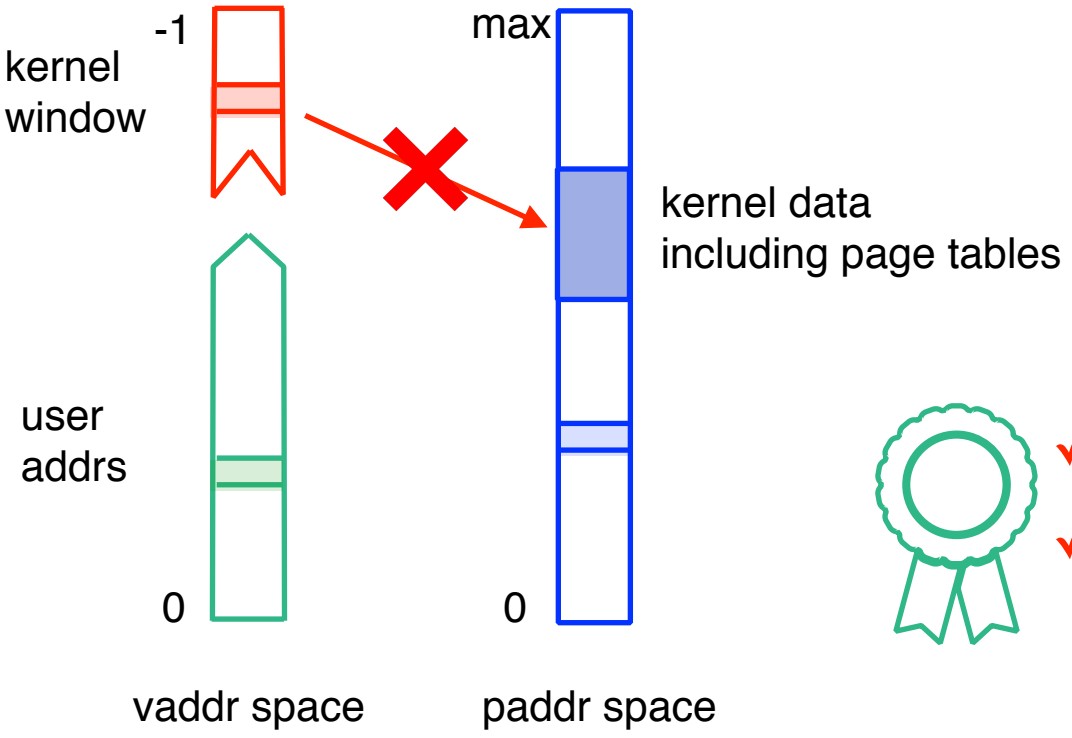

✓TLB remains consistent

✓reduction to
standard Hoare logic

Reduction Theorems

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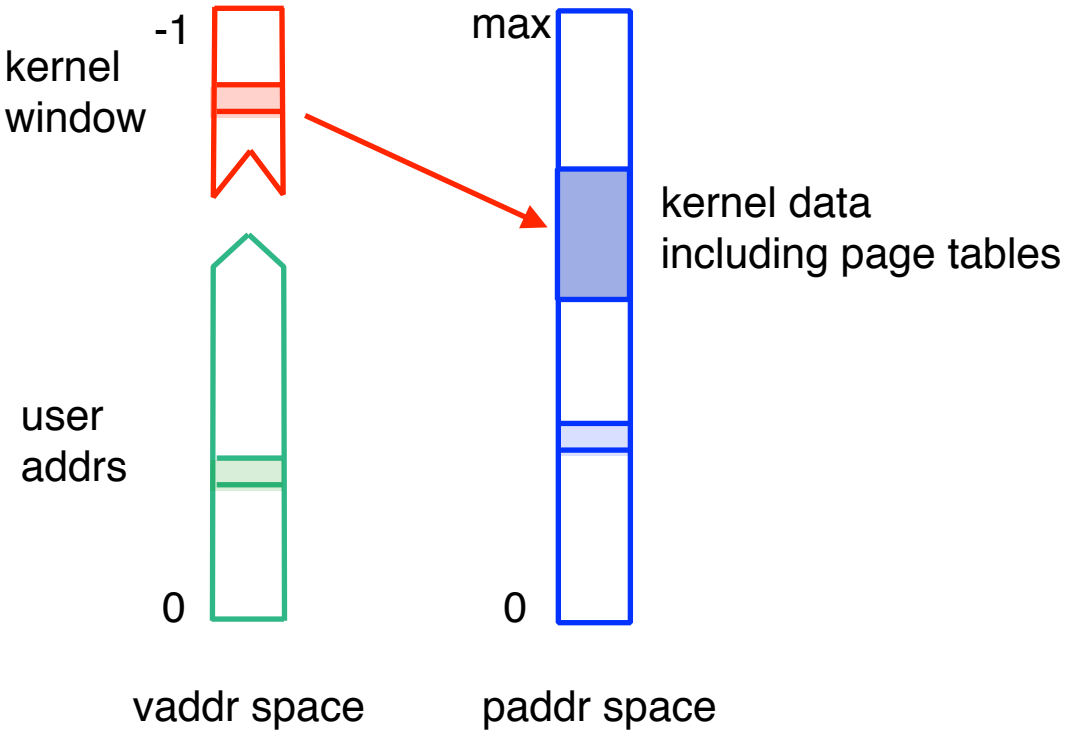

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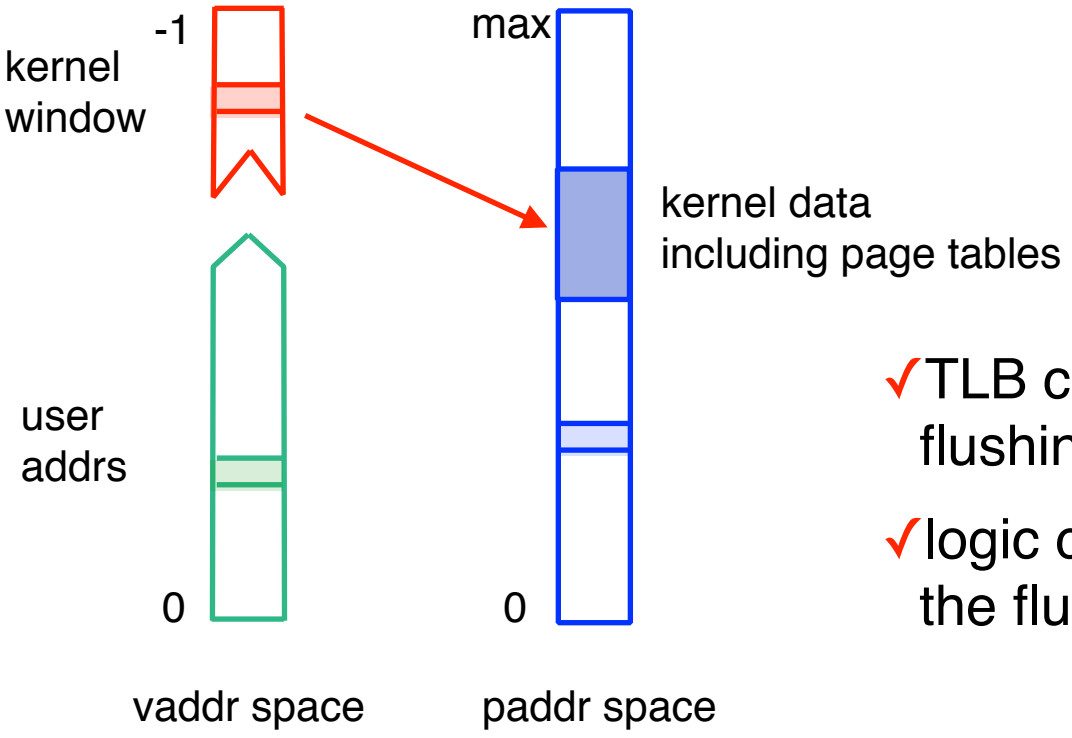

✓TLB consistency is regained by flushing the entries

✓logic correctly identifies when the flush is due

Contributions

- TLB-aware program logic in Isabelle/HOL
  - sound abstraction of ARMv7-style MMU
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  - TLB-aware Hoare logic rules

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Context Switch

- Operations — updating the
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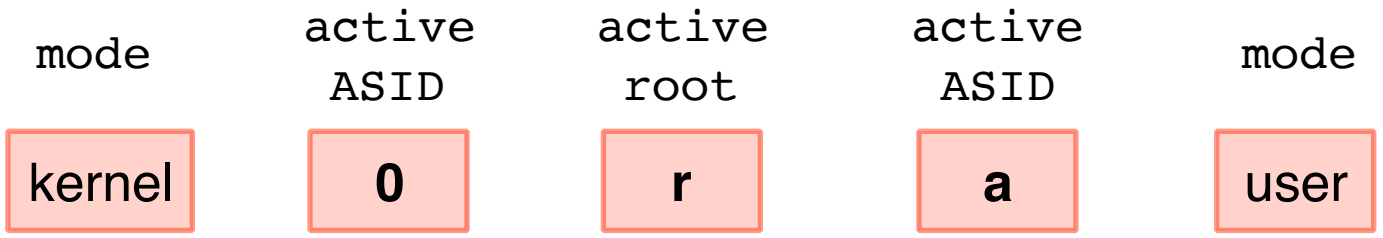

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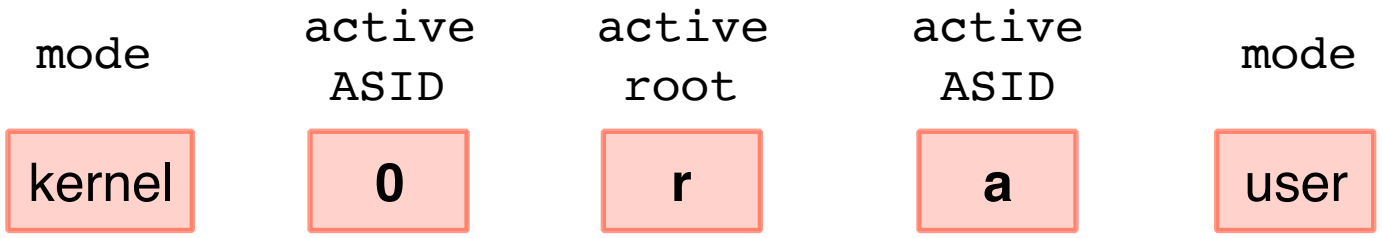

logic can prove that
assigned ASIDs remain consistent

Taken Together

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- simplicity of the logic and memory model
- reduction to Hoare logic for most use-cases

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more in the paper:

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Questions

Reduction Theorems

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$$\texttt{Addr vp} \in \texttt{kernel\_safe s} \wedge \texttt{k\_phy\_ad vp} \notin \texttt{kernel\_data\_area s} \wedge$$
$$\texttt{safe\_set (kernel\_safe s) s}\ |\!\}$$

```
lval ::= rval
```

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Context Switch

- Operations —
  - update root register to `root r`, then
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- ARMv7-A manual's recommended sequence

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